Sigma-Delta A/D Modulator Design in a Pre-Diffused Digital Array Using the Principle of Trapezoidal Association of Transistors

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Abstract

This paper presents analog semi-custom design and the advantages of using the Trapezoidal Association of Transistors (TAT) for mixed analog-digital system applications on pre-diffused digital arrays, such as the Sea-Of-Transistors (SOT). TAT emulates the behavior of a single full-custom transistor, which should have an arbitrary geometry, using only a composition of regularly and linearly placed minimum-length transistors in an array like SOT style. TAT transistor achieves an analog performance that is equivalent to the single device. Basic analog building blocks were fabricated. Second-order sigma-delta modulators for specific applications were also implemented using TAT on SOT. Simulation and experimental results are for technologies at 1.0μm and 0.5μm minimum transistor channel lengths.

I. Introduction

Lately, wireless communication and portable systems are driving electronic industries to continuously improve their products, merging different portable devices with additional functions on a single device at very low cost. The up to date trend is to push research progressively towards VLSI/ULSI technologies, since the power consumption becomes an essential design target because of short battery lifetime. Industries must put forward higher quality and cheaper products, bringing them fast into competitive markets. In an attempt to prompt VLSI/ULSI integrated circuits design, the pre-diffused semi-custom arrays are largely employed, which are good alternative to decrease the design turnaround and prototyping time. The silicon area and speed are often larger than its equivalent full-custom version. The designers achieve the design at high level of abstraction and the remaining steps are automated (positioning and routing), using pre-defined cells and IP (Intellectual Property) blocks from the pre-defined libraries.

The advantages of digital signal processing are also well known, however the world is analog and front-end are communication interfaces, between the real world and digital environment are still very much required. These interfaces frequently require basic building blocks known as analog cells or systems, which are the main component blocks for the Analog-to-Digital and Digital-to-Analog converters (ADC and DAC). However, available technologies are not well appropriate for analog applications, and analog technologies are still costly alternative and mixing analog-digital circuits can be prohibitive.

There are a number of performance issues implementing an analog circuit in the environment traditionally dedicated for digital applications. The noise, DC and AC
performances of MOSFETs are poor compared to bipolar devices. The mixed-signal analog-digital placed side-by-side on same silicon chip causes cross-talks and increased noise levels. Even in the traditional methodologies, analog design is not straightforward. The design difficulty increases in the digital technology environment. It demands better device modeling and new design techniques. For analog design, improvements on CAD tools that reflect more accurately the linear and non-linear behavior of the devices, counting also RF behavior and effects are still needed.

The mixed-signal and analog designs in a digital environment are then difficult tasks, as the array is designed to stress the performance requirements of the large digital blocks, that most likely comprise the overwhelming majority of the transistors effectively used in the array in a mixed system-on-a-chip design. It is possible to overcome or improve on these characteristics with a specific discipline for designing the analog blocks on fixed-size transistors. One important discipline is the use of trapezoidal association of transistors. The unitary transistors on this SOT array were designed in such a way to facilitate migration to down-scaled technologies taking into account solely the digital circuits demand for speed (using $L_{\text{min}}$ transistors only) and adequate average digital load drive for local routing. Equivalently, TAT transistor presented in this paper as a cascoded configuration, that is, a self-cascode amplifier without any extra transistor and bias circuits. Comparisons between TAT and Single version are presented for common-source amplifier and folded-cascode OTA as well as a $2^{\text{nd}}$ order Sigma-Delta designed and fabricated in both methodologies.

II. The TAT Transistor Technique

The principle of TAT transistor was demonstrated earlier at the device level by Riccò [3], showing that enlarging the channel width at the drain end of the channel (trapezoidal shape – small source, large drain), shown in Fig. 1a, results in a substantial improvement of the output conductance in saturation mode. Furthermore, Galup-Montoro [2] established that the series-parallel association of discrete transistors emulates an equivalent single transistor. The TAT transistor is the combination of the previous techniques, i.e., a trapezoidal series-parallel association of transistors, shown in Fig. 1b, using only digital-based pre-diffused transistors.

The transistor variable sizes and geometry for electrically equivalent CMOS channel lengths and widths required for analog design is achieved with appropriate association of the unitary transistors available in a SOT array. Details of this technique are better described in [1], [6].

Consider the series transistors, MD and MS at the drain and source ends, as shown in Fig. 1b, respectively. The equivalent conductance (in linear region) is given by an equivalent aspect ratio of the association as [2]:

$$\left(\frac{W}{L}\right)_{\text{eq}} = \left(\frac{W}{L}\right)_D \left(\frac{W}{L}\right)_S$$

2.1

where $(W/L)_D$ and $(W/L)_S$ are respectively the aspect ratios of the top parallel association MD and the bottom parallel association MS transistors. We can rewrite (2.1) as follows:
Figure 1: (a) trapezoidal geometry of a custom MOSFET transistor. (b) Series-parallel association of minimum transistors of the TAT transistor (Self-cascode configuration).

![Trapezoidal geometry and series-parallel association of transistors]

Figure 2: Simulated $V_x \times V_{DS}$ curve characteristic of TAT transistor: ND=17, NS=4, $L_{min}=0.5\mu m$ digital CMOS technology.

![Simulated curve]

\[
\left( \frac{W}{L} \right)_{Eq} = \frac{m}{m+1} \left( \frac{W}{L} \right)_S \tag{2.2}
\]

with:

\[
m = \frac{\left( \frac{W}{L} \right)_D}{\left( \frac{W}{L} \right)_S}, \quad m > 1 \tag{2.3}
\]

is the ratio between MD and MS transistor aspect ratios. Taking into account the limit of the function in (2.2), from $m=1$ to $m \rightarrow \infty$, the TAT transistor aspect ratio will vary between a half of the MS aspect ratio and its physical individual value. Therefore, we must impose an aspect ratio to the MS transistor greater than the required aspect ratio and smaller or equal than twice this value in order to get a trapezoidal association.

Regarding again Fig. 1b, to achieve improvement (decrease) on the output conductance [8], it is indispensable that the channel width of transistor MD be larger than the width of the MS
transistor, as described in [2] and [3]. In fact, MD is obtained by having \( N_D \) unit transistors in parallel and similarly \( N_S \) unit transistors in parallel for MS, where \( N_S \) is smaller than \( N_D \), in order to keep the principle of trapezoidal geometry. The association of the type shown in Fig. 1 is the basic building block for analog design in a digital SOT array.

For general application, the upper transistor MD operates in the saturation region and the intermediate node voltage \( V_x \), Fig. 2, is clamped at a fraction of the pinch-off voltage of the source end of the MD channel. This effectively limits de drain voltage of MS to be the channel saturation voltage for a given \( V_G \), which keeps MS in the linear region. Both transistors MD and MS have the same gate voltage. Hence, they also have the same channel pinch-off voltage [9], [10], therefore for both MD and MS in strong inversion, considering MD is saturated, \( V_x \) is given by:

\[
V_x = \left[ 1 - \frac{1}{\sqrt{1 + N_D/N_S}} \right] V_P
\]

where \( V_P \) is the pinch-off voltage of the TAT transistor. The expression 2.4 shows clearly the advantage of the TAT to be trapezoidal, i.e., \( V_x \) approaches to \( V_P \). Since the transconductance of TAT is the transconductance of MS transistor (shown later) and MS is in linear region (onset to saturation), the transconductance is directly proportional to the drain-to-source voltage of MS or \( V_x \).

The MD and MS are the equivalent transistors obtained by several unit transistors physically laid out in parallel. Therefore, the equivalent threshold voltage is in fact an averaging over many unit transistor threshold voltages. This averaging in fact compensates the higher spread of \( V_T \) for minimum lengths. Offset voltages should improve by using such composite TAT transistors in deep sub-micron circuits.

The TAT is trapezoidal and channel lengths are the same for both MD and MS transistors (only the electrically equivalent \( L_{eq} \) of TAT is variable). Then, transistor MD is always made wider than transistor MS and its width is not the minimum and the threshold voltage of MS will not be larger than that of MD, given the body effect present. Additionally the TAT association can be used in several analog low voltage applications because it works as an intrinsic self-cascode circuit, a loosely controlled cascode. Normally, a second gate bias for MD is required for a traditional cascode operation.

Improvement, i.e. reduction, on the effective output conductance is effectively achieved for a TAT on SOT array, because a TAT transistor is similar to the traditional cascaded transistors. Then the output conductance is given by traditional expression:

\[
g_o \equiv g_{ds_{MD}} \cdot \frac{g_{ds_{MD}}}{g_{ms_{MD}}} \Rightarrow r_o \equiv r_{ds_{MS}} \cdot \left( r_{ds_{MD}} \cdot g_{ms_{MD}} \right)
\]

From 2.5, the output conductance of MD \( g_{dsMD} \) is represented by a large value, typical of the worst-case minimum channel length transistor, which is effectively reduced by the transconductance of MD. The effective transconductance of TAT transistor is given by:
Figure 3: Experimental output conductance at $V_G=1V$, $V_G=3V$ and $5V$ for TAT and 1.0μm Digital CMOS technology: (a) L=5μm, W=30μm, W/L=6 (ND=12, NS=3, unitary W/L=2.5/1.0). (b) L=5μm, W=170μm, W/L=34 (ND=17, NS=4, unitary W/L=10.5/1.0).

According to 2.6, the transconductance of TAT is determined mainly by the transconductance of MS transistor. Hence, to improve overall TAT characteristics one needs to increase the MS transconductance and improvement on the effective output conductance one has to increase mainly the output impedance or MD transconductance. Thus, the transistor MD mainly determines the output conductance and transistor MS determines the transconductance of the TAT transistor.

In Fig. 3 is plotted the experimental output conductance for TAT transistors with channel length L=5μm and two different widths W=170μm and W=30μm compared to the equivalent full-custom single transistors. It shows clearly that at strong inversion and saturation region the output conductance of the TAT is smaller. At higher gate drive (5V) it is remarkable that the minimum-L TAT transistor achieves a lower $g_{ds}$ in saturation region as the long channel (L=5μm drawn) length devices. At lower gate drive (1V) the short channel effects of $V_T$ reduction and Drain Induced Barrier Lowering (DIBL) combine to give a larger $g_{ds}$ both in conduction and saturation regions. In the saturation region, the output conductance is about the same with respect to its long channel equivalence at higher gate drive.

The total equivalent noise power at the input present in the TAT transistor is given by:

$$V_{n_{ext}}^2 = \left\{ \frac{ND}{NS} \cdot \left\langle \frac{g_{mGS}}{g_{mDS}} \right\rangle \right\} + \left\langle \frac{1}{NS} \right\rangle \cdot V_{n_g}^2 + \left\langle \frac{ND}{NS} \cdot \left\langle \frac{g_{mGS}}{g_{mDS}} \right\rangle \right\} \cdot \left( I_{n_{ext}}^2 \right)_{MD} + \left\langle \frac{NS}{NS} \cdot \left\langle \frac{g_{mGS}}{g_{mDS}} \right\rangle \right\} \cdot \left( I_{n_{ext}}^2 \right)_{MS}$$

where ND and NS are the number of unitary transistors that set up the MD and MS transistors, respectively, and $V_{n_g}^2$ and $I_{n_g}^2$ are the flicker noise and thermal noise of each unitary

\[
\begin{align*}
V_{n_{ext}}^2 &= \left\{ \frac{ND}{NS} \cdot \left\langle \frac{g_{mGS}}{g_{mDS}} \right\rangle \right\} + \left\langle \frac{1}{NS} \right\rangle \cdot V_{n_g}^2 + \left\langle \frac{ND}{NS} \cdot \left\langle \frac{g_{mGS}}{g_{mDS}} \right\rangle \right\} \cdot \left( I_{n_{ext}}^2 \right)_{MD} + \left\langle \frac{NS}{NS} \cdot \left\langle \frac{g_{mGS}}{g_{mDS}} \right\rangle \right\} \cdot \left( I_{n_{ext}}^2 \right)_{MS}
\end{align*}
\]
transistor. Comparing above expression to the equivalent single transistor, TAT transistor is noisier. Electrical simulation and experimental results (for the OTAs) have demonstrated that thermal noise is similar, however flicker noise is larger for TAT, which can be minimized increasing the transconductance of MS (or TAT). The same noise analysis can be extended to the circuits and it is shown in next section.

III. Basic Analog Circuits Using TATs

![Small signal model of TAT transistor with body effect.](image)

Table 1: Comparator simulated performance designed in 0.5μm digital CMOS technology.

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<thead>
<tr>
<th></th>
<th>Full-Custom</th>
<th>SOT</th>
</tr>
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<tbody>
<tr>
<td>Vdd</td>
<td>3V</td>
<td>3V</td>
</tr>
<tr>
<td>C_L</td>
<td>10pF</td>
<td>10pF</td>
</tr>
<tr>
<td>f_max</td>
<td>70MHz</td>
<td>40MHz</td>
</tr>
<tr>
<td>V_os</td>
<td>10mV</td>
<td>18mV</td>
</tr>
<tr>
<td>P_diss</td>
<td>0.1mW @ 14.3MHz</td>
<td>0.13mW @ 14.3MHz</td>
</tr>
<tr>
<td>I_tail</td>
<td>84μA</td>
<td>93μA</td>
</tr>
</tbody>
</table>

The main parasitic capacitances in TAT transistor are the gate-source capacitance from MD transistor (in saturation) and from MS transistor (in conduction) is the gate-source and gate-drain capacitance, shown in Fig. 4. The combination of parasitic capacitances is larger for the TAT than in its equivalent single transistor. The presence of one more node in the TAT (poles) increases the total parasitic capacitance seen at the input. Nevertheless, due to the cascode effect the gain bandwidth is similar to the single transistor one. Indeed, the product gain-bandwidth is increased by the cascode effect of the TAT. The electrical simulations in Fig. 5 show clearly that for the common-source amplifiers with PMOS current source. The channel lengths, widths and W/L ratios are exactly same values for both TAT and Single transistor for better comparison purposes, as indicated in the figure caption.

Fig. 6a shows the total equivalent noise power source at the input of common source amplifiers. It is clearly noted that the flicker noise is almost 5 times larger with TAT transistors.

A track-and-latch comparator, shown in Fig. 7a, was designed due to its higher speed operation. In order to hold and increase output fan-out, the signal compared and memorized during sampling time, the comparator must be followed by a latch type D at the output. In Tables 1, the simulated performance reached by the comparator is summarized. The
technology parameters are for HP 0.5µm 3 metal digital CMOS technology and were used Smartspice and Hspice electrical simulators with Level 49, which includes noise parameters (1/f and thermal noises).

<table>
<thead>
<tr>
<th></th>
<th>Full-custom</th>
<th>SOT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_v$ (db)</td>
<td>64.5</td>
<td>62.9</td>
</tr>
<tr>
<td>GBW(MHz) @ $C_l$(pF)</td>
<td>0.186</td>
<td>0.514</td>
</tr>
<tr>
<td>GBW @ 50pF</td>
<td>0.257</td>
<td>0.499</td>
</tr>
<tr>
<td>$V_{os}$(mV)</td>
<td>+30</td>
<td>-15</td>
</tr>
<tr>
<td>SR (V/µs) @ $C_l$(pF)</td>
<td>0.42</td>
<td>1.10</td>
</tr>
<tr>
<td>PM ($)</td>
<td>79.4</td>
<td>51.7</td>
</tr>
<tr>
<td>$V_{os max}$(V)</td>
<td>+1.1/-0.7</td>
<td>+0.9/-0.9</td>
</tr>
</tbody>
</table>

Table 2: OTAs measured performance designed in 1.0µm digital CMOS technology.

Figure 5: Gain and Phase margin. HSpice simulation of a common-source amplifier using TAT (solid) and Single (dotted) transistors ($W/L_{eq}=106/1.9$) for 0.5µm digital CMOS technology.

Figure 6: Total equivalent noise power: (a) HSpice simulation of a common-source amplifier using TAT (solid) and Single (dotted) transistors ($W/L_{eq}=106/1.9$) for 0.5µm digital CMOS technology. (b) Experimental results from folded-cascode OTA designed in both SOT and full-custom methodologies for 1.0µm CMOS technology.
Figure 7: (a) Track-Latch Comparator. (b) Folded-Cascode OTA.

Figure 8: Die photo: OTA on SOT array (left) and same OTA in full-custom (right).

A single-ended folded-cascode OTA - Fig. 7b - in both SOT (using TAT transistors) and full-custom methodology [6], [7] were also designed to allow better performance comparisons. In Fig. 8 the die photos of the folded-cascode are shown. In Table 2 the results for electrical simulations and experimental measurements are summarized for both SOT array and full-custom OTAs. The load capacitances were estimated from electrical simulation of expected output current and measured slew-rate. It is worth noting that the SOT with TAT transistors version of OTA has similar (or 1.9X times higher) gain-bandwidth. It is expected because the TAT transistor is an intrinsic cascode (self-cascode pointed out previously).

The offset voltage in the SOT version of OTA is smaller than the full-custom version of OTA due to its better intrinsic layout configuration, that is, naturally the TAT transistors are very similar to the interdigitated layout technique that is widely used in full-custom layouts. The total noise power spectral densities measured in both OTAs are shown in Fig. 6b. The flicker noise in both are large due to its dependence on the OTA input differential pair [4], [5]. In this design, these differential pair geometries are smaller than usual. The thermal noise in the SOT version of OTA is almost similar (slightly higher) to its equivalent version in full-custom, as already predicted previously.

An ADC system was fabricated, in 0.5μm digital CMOS technology, using the building blocks implemented previously. A fully differential OTA (not shown here) was implemented in order to be compatible to the 2nd order fully differential Sigma-Delta A/D converter (shown in Fig. 9) for a specific application, i.e., for a multi-standard wireless communications. This converter was fabricated in both full-custom and SOT methodologies. Testing procedures are under investigations. Pictures of the integrated circuits containing A/D system are shown in Fig. 10.
Figure 9: Fully differential 2\textsuperscript{nd}-Order Sigma-Delta Modulator architecture.

Figure 10: A 2\textsuperscript{nd} order Sigma-Delta A/D converter fabricated in 0.5\textmu m digital CMOS technology: (a) Full-custom. (b) SOT methodology.

IV. Conclusion

This paper demonstrated that the TAT technique could be used in analog circuit applications without major penalties. One has to deal with the demonstrated noise figures; it is noisier than the single transistor counterpart. However, using a large number $N_D$ of minimum-size transistors in the TAT, the worse characteristics with respect to noise can be compensated, while keeping the same equivalent $W/L$. The TAT transistors, as shown herein, are not restricted only for semi-custom arrays. It can be used advantageously even in full-custom analog integrated circuits, as shown by the sub-circuits and sigma-delta converter implemented in SOT using TAT.

Even though the total noise is larger and some natural limitations exist, the TAT transistors in SOT methodology present good performance. It is a good trade-off, for a given application, between performance and cost and design time turn around.
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V. Reference


