PTAT Voltage Generator based on an MOS Voltage Divider

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ABSTRACT

An MOS-only, proportional to absolute temperature (PTAT) voltage generator capable of operation in the whole range of inversion levels is presented. We perform a theoretical analysis based on the ACM model which is successfully compared to experimental data. PTAT voltages up to hundreds of milivolts at room temperature can be easily obtained.

Keywords: PTAT voltage, compact MOSFET model, CMOS analog integrated circuits, temperature sensors

1 INTRODUCTION

Proportional to absolute temperature (PTAT) voltage generators are needed in several modules, mainly voltage references and temperature sensors.

The design of this kind of circuit must rely on accurate device modelling, specially regarding temperature variation. Although charge-based compact models are already well established, little has been published on their use as design tools for variable operating temperature design.

This paper presents the use of an MOS divider as a PTAT voltage generator. Section 2 introduces the notation while reviewing the ACM model. In section 3 we apply the model to analyze the described circuits. Section 4 compares the theoretical results to measurements on a circuit prototype. Finally, we draw some conclusions on section 5.

2 THE ACM MODEL

The ACM (Advanced Compact MOSFET) model [1] [2] has proved to be an important tool for circuit design due to its accurate modelling of MOSFETs through all inversion levels.

In ACM, the drain current of a long-channel MOSFET is expressed as

$$I_D = S\, I_{SQ}\,(i_f - i_r) \tag{1}$$

where i_f and i_r are the forward and reverse inversion coefficients and $S = W/L$, W and L are the effective width and length of the MOSFET, respectively. I_{SQ} is the sheet normalization current, defined as

$$I_{SQ} \;=\; \frac{1}{2}\, n\, \mu C'_{ox}\, \phi_t^2 \tag{2}$$

where n is the subthreshold slope factor, μ is the channel effective mobility (both slightly dependent on the gate voltage V_G), C'_{ox} is the gate capacitance per unit area and $\phi_t = kT/q$ is the thermal voltage, k is Boltzmann's constant, q is the electronic charge, and T is the absolute temperature.

The inversion coefficients (i_f, i_r) are related to the device terminal voltages by [1] [2]

$$\frac{V_P - V_{S(D)}}{\phi_t} \;=\; \mathcal{F}\left(i_{f(r)}\right) \;=\; \sqrt{1 + i_{f(r)}} \;-\; 2 \;+\; \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{3}$$

where V_S and V_D are the source and drain voltages (all terminal voltages are referenced to the transistor bulk). V_P is the pinch-off voltage [1] [2], dependent on V_G approximately as $V_P = (V_G - V_T)/n$, where V_T is the threshold voltage. The transistor operates in weak inversion for $i_f < 1$ and in strong inversion for $i_f > 100$.

3 CIRCUIT ANALYSIS

The MOS divider in Fig. 1 is well known for its PTAT output when both transistors operate in weak inversion [3]. The result has recently been extended to strong inversion when the bias current has a special temperature dependence [4]. In this section we show that the MOS divider output is PTAT for any inversion range, including moderate inversion, when biased by a current in such a way that the inversion level remains constant over temperature.

We will first review a couple of general expressions that will be used later on.

When two MOS transistors (M1 and M2) share the same gate voltage (V_G), both have the same pinch-off voltage (V_P). Applying Eq. 3 to both source terminals yields

$$V_{S2} \;-\; V_{S1} \;=\; \phi_t \left[\mathcal{F}\left(i_{f1}\right) \;-\; \mathcal{F}\left(i_{f2}\right)\right] \tag{4}$$

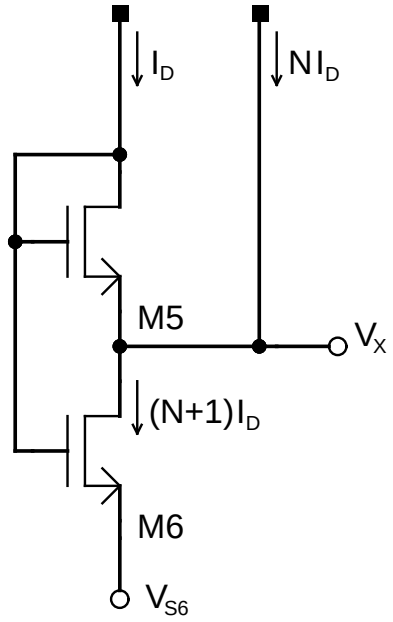

Figure 1: PTAT generating MOS divider

This simple result is independent of the circuit topology as long as the gate terminals are tied together.

Applying Eq. 3 to the drain and source terminals of a single MOSFET results in the following expression for its drain-source voltage:

$$V_{DS} \;=\; \phi_t \left[\mathcal{F}\left(i_f\right) \;-\; \mathcal{F}\left(i_r\right)\right] \tag{5}$$

3.1 Constant Inversion Level Bias Current Generator

A constant inversion level is obtained through a particular temperature dependence of the bias current which, nevertheless, is very easy to obtain with a simple circuit (Fig. 2). This topology was first proposed in [5] [6] with a limited operating range in terms of inversion coefficients. More recently it was partially extended, in a similar circuit, in [7].

In the circuit of Fig. 2, the current mirror imposes proportional currents through all branches. In order to simplify the analysis, we will consider all of them equal. As M3 and M4 share the same V_G and V_S, then $i_{f3} = i_{f4}$. Transistors M1 through M3 are saturated, so $i_f \gg i_r$ in each of them. Thus,

$$S_1 i_{f1} \;=\; S_2 i_{f2} \;=\; S_3 i_{f4} \;=\; S_4 \left(i_{f4} - i_{r4}\right) \tag{6}$$

Transistors M1 and M2 determine the voltage through M4 (V_{DS4}) which operates in the triode region (substituting a resistor) and fixes the current through M2. The current mirror imposes a copy of this current through M1 and M3. As the elements are non-linear there is an equilibrium point which can be found by applying Eq. 4

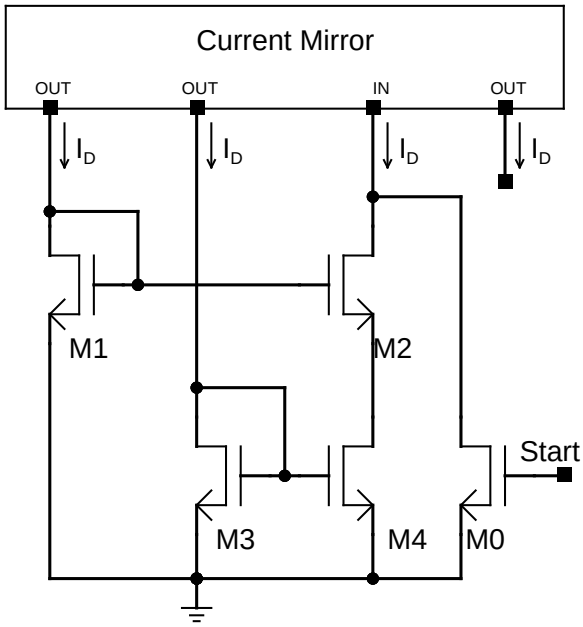

Figure 2: MOS-only constant inversion level bias generator

to M1-M2 and Eq. 5 to M4. Thus,

$$\mathcal{F}\left(i_{f1}\right) \;-\; \mathcal{F}\left(i_{f2}\right) \;=\; \mathcal{F}\left(i_{f4}\right) \;-\; \mathcal{F}\left(i_{r4}\right) \tag{7}$$

The expressions in Eq. 6 and Eq. 7 are four equations that determine i_{f1}, i_{f2}, $i_{f4}(= i_{f3})$ and i_{r4}. The inversion coefficients must be positive which imposes the condition $S_4 > S_3$.

The only parameters in the equations are the geometrical ones $(S_1 - S_4)$, thus, the inversion coefficients are constant, independent of the temperature, and the branch currents are proportional to I_{SQ}. Therefore, M1-M4 together with the current mirror constitute an MOS-only constant-inversion-level current generator.

Some kind of start circuitry is needed to avoid the trivial solution of Eq. 7. This problem is easily solved by imposing a transient current, higher than steady-state, with an externally controlled start transistor (M0).

3.2 MOS Divider

The current generator can be used to bias the MOS divider (M5 and M6) as shown in Fig. 1. Besides the main bias I_D, a second (optional) current (N I_D) is included.

As both transistors share the same gate voltage and the source of M5 is tied to the drain of M6, then $i_{f5} = i_{r6}$. M5 is saturated, so $i_{f5} \gg i_{r5}$. Thus,

$$\begin{aligned} I_{D5} \;&=\; I_D \;=\; S_5\, I_{SQ}\, i_{f5}\,, \\ I_{D6} \;&=\; (N+1) I_D \;=\; S_6\, I_{SQ}\left(i_{f6} - i_{f5}\right) \end{aligned} \tag{8}$$

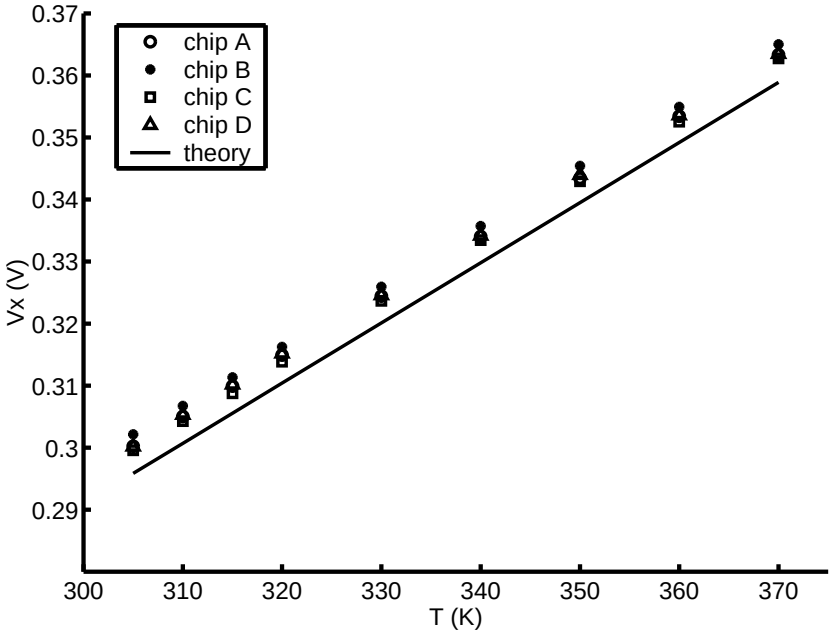

Figure 3: Experimental and theoretical data of the PTAT voltage generator

which results in

$$i_{f6} \;=\; G\, i_{f5}\,, \quad \text{where} \quad G \;=\; \left[1 \;+\; (N+1)\,\frac{S_5}{S_6}\right] \qquad (9)$$

Applying Eq. 5 to M6 and using Eq. 9 we get

$$\frac{V_X \;-\; V_{S6}}{\phi_t} \;=\; \mathcal{F}\,(G\, i_{f5}) \;-\; \mathcal{F}\,(i_{f5}) \qquad (10)$$

The bias generator imposes that I_D is proportional to I_{SQ}, so (Eq. 8) i_{f5} is constant. As G depends only on geometrical parameters, then the right hand side of Eq. 10 is also constant, which makes $V_X - V_{S6}$ PTAT. If V_{S6} is PTAT (including the frequent case $V_{S6} = 0$), then V_X is also PTAT.

A closer look to the circuit should consider that I_{SQ} exhibits some dependence on the V_G of each transistor through n and μ. In the precedent analysis, all sheet normalization currents (I_{SQ}) were supposed equal. Taking this effect into account makes the actual slope different than predicted. As the dependence of I_{SQ} with V_G is very weak, this variation is very slight.

The sensitivity (temperature slope) of the PTAT generator can be varied by adjusting i_{f5} and i_{f6} through I_D, N, S_5 and S_6. In order to get a steep slope we need $G \gg 1$. If, additionally, the total current must be kept low then it usually results $S_6 < 1$ and the circuit area increases as $1/S_6$. Thus, Eq. 9 expresses a tradeoff between area and consumption.

4 EXPERIMENT

The theoretical results were checked on a circuit comprising a constant inversion level bias generator and an MOS divider fabricated in a standard $0.8\,\mu$m CMOS technology. The MOS divider was designed with $N = 0$ while M5 was drawn as $2\,\mu\text{m}/58\,\mu\text{m}$ and M6 was implemented as the series of 24 unit transistors identical to M5. These configuration results in $G = 25$.

The circuit was measured in a custom oven whose temperature was controlled to $\pm 10\,$mK. At the lowest available temperature (305 K) the bias current was around 7 nA, thus obtaining inversion coefficient values around $i_{f5} = 6$ and $i_{f6} = 150$ corresponding, respectively, to operation in moderate and strong inversion.

A combined analysis of the bias generator and the MOS divider shows that the temperature slope depends only on the geometry (S_1 to S_6). Considering typical technology values to obtain effective sizes from drawn geometries yields a $0.97\,$mV/K slope which is shown as a solid line in Fig. 3.

This result is compared to data from the four measured chips (A to D) which are shown as dots in Fig. 3.

5 CONCLUSION

We have presented a simple PTAT voltage generator based on an MOS voltage divider driven by a MOSFET-only, constant inversion level, bias current generator. The sensitivity of the PTAT voltage can be adjusted by means of both the inversion level and a current multiplication factor.

PTAT voltages up to hundreds of mV at room temperature can be achieved with a MOSFET-only circuit, an interesting property not only for application as a temperature sensor but also in voltage references, for

resistorless compensation of the negative temperature coefficient of bipolar transistors.

Our theory is supported by experimental data from a circuit which combines transistors operating in moderate and strong inversion levels.

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