High Precision Load Current Sensing Using On-Line Calibration of Trace Resistance

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Abstract—A method for the on-line calibration of a circuit board trace resistance at the output of a buck converter is described. The input current is measured with a precision resistor and processed to obtain a dc reference for the output current. The voltage drop across a trace resistance at the output is amplified with a gain that is adaptively adjusted to match the dc reference. This method is applied to obtain an accurate and high-bandwidth measurement of the load current in the modern microprocessor voltage regulator application (VRM), thus enabling an accurate dc load-line regulation as well as a fast transient response. Experimental results show an accuracy well within the tolerance band of this application, and exceeding all other popular methods.

Index Terms—Adaptive voltage positioning (AVP), current sensing, dc–dc converters, voltage regulator for modern microprocessors (VRMs).

I. INTRODUCTION

VOLTAGE regulators for modern microprocessors (VRMs) pose unprecedented demands on dc–dc power converters, in terms of regulation, bandwidth, and cost [1]. Adaptive voltage positioning (AVP), also known as load-line regulation, was adopted as an effective technique to reduce the amount of capacitance at the output [2]. This technique requires the output voltage to change with the load current, as if the output impedance of the power converter were a resistor of small value (of about 1 mΩ). The controller can be designed to make the effective closed-loop output impedance resistive, or to meet another desired specification, over a wide frequency range, by processing the output current information [2], [3]. For this reason, and due to the tight regulation window required by the application, a precise and high-bandwidth measure of the output current is needed.

Existing current-sensing methods are shown and compared in Table I, [4], [5], together with the method proposed in this paper. The table indicates the main features of each method from the VRM application point of view. Current transformers are used in some applications with current-mode control, but they have the disadvantage that they don’t provide dc information. There are techniques to reconstruct the dc value of the current by sensing multiple branches of the circuit [6], but the complexity and cost of the solution is very high. Design considerations on current transformer design can be found in [7], [8]. Hall effect sensors are accurate and efficient options for some applications, but they have a moderate bandwidth and a prohibitive cost for the VRM application. An example of a hall sensor design can be found in [9]. A sense resistor connected in series with the load is a popular current sensing method for lower-current applications, but the efficiency is very low for high-current, low-voltage applications. $R_{DS}$ sensing is an efficient method but its accuracy is low due to the uncertainty in the metal oxide semiconductor field effect transistor (MOSFET) ON-resistance value; in some multi-phase commercial applications it is used for current balancing. Inductor sensing is the most popular method and is described in more detail below. The SENSEFET method integrates a sensing MOSFET in parallel with the power MOSFETs and can provide an accurate and efficient current measurement. However, the method is not popular for VRM applications because integration of the sensing element with the power switch, although not costly by itself, implies the use of special discrete components and this solution is not cost-effective, with currently available parts. Some design issues around an integrated CMOS current-sensing circuit and a practical design achieving 4% accuracy for lower power applications are discussed in [10], [11]. Input-side current sensing has been proposed for this application and it was shown that with a compensation circuit it can achieve AVP within the tolerance band [12]. However, the correlation between the input current and the output current is valid only at low frequencies. In the proposed method, instead, the input current is used as a means to calibrate the output trace resistance, which can provide much better dynamic response during fast transients.

Other methods have been proposed but are not used commercially. An on-line calibration method for MOSFET $R_{DS}$ sensing that requires additional power train components, was described in [13]. An observer-based approach requiring intensive numerical processing was reported in [14]. A sensorless approach similar to inductor sensing was proposed in [15].

For efficiency, cost, and relative accuracy, inductor sensing is the preferred method at the present time [1]. The method is illustrated in Fig. 1. The relationship between the capacitor voltage and the inductor current in the frequency domain is

\[
I_L = \frac{V_{sw} - V_O}{Ls + R_{dcr}} = \frac{V_{sw} - V_O}{\frac{1}{R_{dcr}} s + 1} \quad (1)
\]

\[
V_C = \frac{V_{sw} - V_O}{RCS + 1} \quad (2)
\]
If $R_C = (L)/(R_{dkr})$, then

$$V_C = R_{dkr}I_L.$$  \(3\)

It can be appreciated that this method has the disadvantage that both the effective series resistance $R_{dkr}$ and the $L/R$ time constant of the inductor need to be known and tracked as they change with temperature. A discussion of these issues can be found in [16].

Most of the methods described above sense the inductor current, which has the same dc value as the output current, and tracks it well up to the closed-loop bandwidth of the converter, but it is not useful for fast load transients. For this reason, in Table I the bandwidth of methods that sense the inductor or switch current are set to medium, and only the methods that sense the output current are set to high.

In designs with electrolytic capacitors, the output capacitor’s ESR is chosen to be equal to the desired output impedance, as given by the load-line specification. This allows the converter to follow the load-line ideally at an arbitrary high bandwidth [2]. However, if ceramic capacitors are used the ESR is substantially lower than the load-line impedance rendering the previous design method impractical. The concept of generalized load-line was introduced in [17] as a practical design objective for VRM systems with ceramic capacitors. The bandwidth in such a system is given by the time constant $\tau = R_{LLL}C_0$ where $R_{LLL}$ is the desired load-line and $C_0$ is the output capacitor value. In some cases it could be very difficult to follow the load-line over this frequency range, especially as $C_0$ is decreased to reduce costs. In order to enhance load-line tracking without pushing the feedback bandwidth close to instability, output current feedforward was proposed [17]. In this case, the inductor current information is not useful by itself and the load current must be sensed.

In [17], the authors used inductor sensing together with an analogous technique to sense the output capacitor current, and combined both to obtain the output current. Thus, the method used poses the same practical challenges as inductor sensing.

The objective of this work is to develop a current sensing method with the following characteristics:

1) Output current sensing. By sensing the output current, a high bandwidth signal is obtained that can be used in an output current feedforward scheme to improve the transient response of the system.

2) Accuracy of 1%. An inductor sensing accuracy of 7% can be achieved at a reasonable cost today [18]. This means that at 100 A in a 1 mΩ load-line the voltage error is ±7 mV. As a consequence, the designer has to assign an inductor sensing error budget of 14 mV out of a 40 mV tolerance band (TOB) [1]. With a more accurate sensing method, achieving 1% accuracy, the error budget could be reduced to 2 mV, thus relaxing the constraints for other circuit components.

3) Efficient. In high-current applications such as in the VRM, the designer cannot afford to put additional components in the power train.

4) Low cost. This is always a desired objective, especially in commoditized applications such as the VRM. In practice this means, among other things: reduced bill of materials (BOM), low pin-count, little extra IC complexity.

In this paper, a method that approaches these ideal conditions is presented. The method senses the output current by using the output trace resistance (or any parasitic resistance at the output of the converter) as a sensing element. The value of the trace resistance is calibrated on-line by a slow estimation loop. The estimation algorithm is based on the dc correspondence between the output current and the input current. The latter is accurately measured with a sense resistor and used as a reference. This method can achieve high-accuracy and high-bandwidth measurement of the output current with a small efficiency penalty due to the input-side resistor. Further, the measured input current may be useful for control purposes.

This solution has two parts in the signal path: an uncertain sense resistance that is calibrated on-line and a current sense amplifier. This paper mainly focuses on the calibrated sense re-
sistance. The sense amplifier can be purchased or designed in the native IC process. The specifications for this amplifier are discussed in the next section.

This paper is organized as follows. The output current sensing method is described in Section II. A detailed error analysis is presented in Section III, as well as some techniques to improve the accuracy. Finally, experimental results are reported in Section IV.

II. METHOD DESCRIPTION

Fig. 2 shows a buck converter. The output trace resistance is shown explicitly as element $R_t$. The input current $I_{in}$ is measured by placing a sense resistor before the input capacitor. Usually an inductor is located at this place as a choke, so this current is mostly dc and free of high frequency noise. In steady-state, the average current through the input capacitor is zero, so the average current through the high-side switch is being effectively measured. This current can be ideally expressed as $uI_L$, where $I_L(t)$ is the inductor current

$$u(t) = \begin{cases} 1, & \text{if } S_1 \text{ is ON} \\ 0, & \text{if } S_1 \text{ is OFF} \end{cases}$$

(4)

It can also be argued that the average current through the output capacitor is zero, so the average inductor current is equal to the average output current. Then

$$\langle I_{in} \rangle = \langle uI_L \rangle$$

(5)

$$\langle I_L \rangle = \langle I_o \rangle$$

(6)

where $\langle \cdot \rangle$ indicates the dc or average component of the signal. In steady-state and in continuous conduction mode (CCM)

$$\langle uI_L \rangle = \langle uI_o \rangle$$

(7)

as illustrated in Fig. 3. Therefore, it can be concluded that

$$\langle I_{in} \rangle = \langle uI_o \rangle.$$  

(8)

This relationship establishes the basis of the on-line calibration algorithm. In Fig. 4 a block diagram of the estimation loop is shown. The current sense amplifier (CSA) measures the voltage drop on the trace resistance $(V_o - V_s)$. Its output is the estimated current $\hat{I}_o$. This value is multiplied by the function $u(t)$, simulating the operation of the top switch. The difference between this signal and the input current $I_{in}$ is sent to the input of an integrator, whose output sets the gain of the CSA, therefore closing the loop and forcing the integrator to converge to the correct gain. If the gain is too low, the input of the integrator will be positive and the gain will increase, and vice versa. The loop will converge to set the gain such that the condition expressed in (8) is met, therefore achieving the desired result $\hat{I}_o = I_o$. The bandwidth of this adaptive tuning loop should be slow enough as to average-out the effect of switching and load transients, but fast enough to allow for tracking temperature changes. This gives a practical criteria to set the gain of the loop. A low bandwidth is also needed to guarantee the stability of the adaptive loop. Notice that, although the adaptation loop is slow, the actual measurement of the output current is high-bandwidth, because it is given by the voltage drop $V_o - V_s$ across the passive trace resistance amplified with a variable gain amplifier.

The magnitude of the differential voltage $V_o - V_s$ has to be such that the signal can be resolved. This means that there is a trade-off between the signal amplitude and the power loss.
due to the trace resistance. This trade-off results in the selection of a specific PCB layout and impacts the characteristics of the CSA. As an example, consider a representative example of a VRM with a maximum load current equal to 100 A, an output voltage equal to 1 V, and a trace resistance of 0.2 mΩ. At the maximum current, the voltage drop \( V_o - V_w \) would be equal to 20 mV. This represents a power loss of 2 W out of 100 W delivered to the load. Since the typical efficiency for this application at full load is in the range of 75–85%, the impact of the power loss due to the trace resistance is acceptable. For a 1% sensing accuracy, it is necessary to resolve 200 μV out of the 20 mV voltage drop. The bandwidth desired for this measurement is on the order of a few megahertz. A CSA with these characteristics (sub-1mV offset and input-referred noise, with a bandwidth well below 100 MHz) is quite feasible with current technology, although it would require an offset cancellation circuit in a CMOS realization and considerable design effort. In this paper, the trade-off between efficiency, cost, accuracy and bandwidth is not discussed further, with the understanding that it needs to be solved by the designer of a specific application.

III. METHOD ANALYSIS

Some of the assumptions made in the previous section are valid only in ideal circuits. First, there are many factors that make (8) only an approximate equation. Second, the PCB trace that goes from the output capacitors to the load behaves as a resistive element only over a certain bandwidth due to parasitic elements. These issues are addressed in the following subsections.

A. Errors Due to Simplified Switching Model

In a practical implementation, (8) is only approximate. The sources of error are described below.

1) Reverse Recovery: Not all the current that goes through the high-side switch flows to the inductor. A correction has to be made to the input current information in order to reflect more accurately the inductor current. Some of the charge that flows through the high-side MOSFET ends up charging/discharging parasitic capacitances and, most importantly, are recombined in the low-side MOSFET’s antiparallel diode (reverse recovery). This effect can be modeled by rewriting (5) as [19, pp. 244–247]

\[
\langle I_{in} \rangle = \langle uI_L \rangle + Qr_{rr}f_s + t_{rr}f_s \langle I_L \rangle \tag{9}
\]

where \( Q_{rr} \) is the reverse recovery charge, \( t_{rr} \) is the reverse recovery time, and \( f_s \) is the switching frequency. This equation includes both the effect of the charge flowing to the diode and the delay in the switching node voltage due to the reverse recovery time. Rearranging terms, approximating \( \langle I_L \rangle \approx \langle I_{in} \rangle/(D) \), and introducing (7), it is concluded that

\[
\langle I_{in} \rangle \left(1 - \frac{t_{rr}f_s}{D} \right) - Q_{rr}f_s = \langle uI_L \rangle \tag{10}
\]

This expression is more accurate than (8), and can be easily contemplated in the estimation circuit of Fig. 4 by introducing a gain factor slightly less than unity. In practice, the constant term \( Q_{rr}f_s \) is very small (comparable to the voltage offset of the amplifiers), so it can be neglected. The gain factor is represented in Fig. 5 by the block with gain \( k = 1 - (t_{rr}f_s)/(D) \). For a representative VRM design, \( k \) is around 0.93. Although the uncertainty on the value of \( t_{rr} \) may be significant, the effect on the overall accuracy is small. For example, a 30% error in \( t_{rr} \) generates a 2.1% error in \( k \). Further, in Section IV it is shown that without any correction, a total error of 4% is achieved, still better than most current sensing methods.

2) Switching Command Delay: The function \( u(t) \) is an idealization of the switching action. In practice, there is a delay between the gate-drive command and the effective switching. This error can be reduced by extracting \( u \) directly from the switching node, and not from the gate-drive command. This implementation is illustrated in Fig. 5 by introducing a hysteretic comparator to sense the switching node voltage.

3) Transients: It is clear that (8) was derived under the assumption of steady-state operation, since it is based on the fact that the average current on the input and output capacitors is zero. However, the output voltage changes with the load due to Adaptive Voltage Positioning (AVP), so some of the current through the inductor goes into charging/discharging the output capacitor during load transients. It can be shown that the effect of transients on the adaptation algorithm is negligible provided that the adaptation is slow enough. The following analysis illustrates how to set bounds on the adaptation loop bandwidth.

Assume there is an output current step \( \Delta I_o \). Then the average inductor current will converge exponentially to the new output current value with time constant equal to \( \tau = R_{LL}C_o \), where \( R_{LL} \) is the load-line value and \( C_o \) is the output capacitor value [17]. During the transient, (6) is not valid, since the difference between \( (I_o) \) and \( (I_L) \) is equal to \( \Delta I_o \exp^{-t/\tau} \). The integral of that difference is \( A_0\Delta I_o \tau \), where \( A_0 \) (in units of rad/S-V) is the gain of the integrator (i.e., the transfer function of the integrator is \( (A_0)/(s) \)). If the relative error due to this transient is bounded, then

\[
\frac{A_0\Delta I_o \tau}{1/R_i} < \epsilon \tag{11}
\]
where $1/R_t$ is the ideal gain of the CSA and $\epsilon$ is the desired relative error. This equation gives the following upper bound on the integrator gain

$$A_0 < \frac{\epsilon}{\Delta I_o \tau R_t}, \quad (12)$$

For a representative VRM [1], $\Delta I_o^{\text{max}} = 100$ A, $\tau = 1\mu$s, and $R_t = 0.3$ m$\Omega$. With $\epsilon = 0.5\%$, then $A_0 = 165 \times 10^3$. The quantity of interest for this calculation is the loop bandwidth, that can be extracted from the circuit of Fig. 5 by linearization. The loop gain can be expressed as

$$H(s) = \frac{A_0}{s} L_o R_t D \quad (13)$$

therefore the loop bandwidth is

$$\omega_{BW} = A_0 L_o R_t D. \quad (14)$$

Notice that the bandwidth depends on the output current. The limitation in the integrator gain gives a bound in the loop bandwidth. For a typical current of 30 A, this bandwidth is

$$\omega_{BW}^{\text{max}} = 148 \text{ rad/s} \quad (15)$$

or equivalently, a time constant of 42 ms. This is fast enough to track any thermal transient.

4) Discontinuous Conduction Mode: The relationship (8) is valid only in CCM. The converter enters Discontinuous Conduction Mode (DCM) at light loads for some architectures. For operation at light load in either CCM or DCM, the state of the integrator and thus the adaptive loop should be frozen. Freezing the state of the integrator is straightforward with a digital integration function. Interrupting the adaptive loop is not a problem since the parameter being estimated is essentially a dc quantity, and the adaptive calibration loop provides excellent accuracy at moderate and high load conditions. Thus, the loop would be frozen with a precisely computed value for the current sense amplifier (CSA) gain. The sense element and the CSA continue to provide full functionality in light load in either CCM or DCM. It is also relevant that for the VRM load-line regulation application, the absolute sensitivity to load current is minimal at light-load conditions.

B. Errors Due to Lumped Resistance Model

The output trace behaves resistively over a certain frequency range, but at high frequencies the parasitics of the PCB trace make the resistive model unrealistic. This imposes a practical limit in the bandwidth of the sensing method. A first-order estimation of the frequency response of two parallel copper plates in a PCB is derived here. Consider a stripline consisting of a pair of rectangular copper plates of length $L$ and width $W$, separated by a dielectric material of thickness $h \ll L, W$ and relative permeability $\mu_r \approx 1$. When a current $I$ flows lengthwise through one of them and returns in the opposite direction through the other, a magnetic field $H = (I)/(W)$ is formed in the dielectric. The magnetic flux is then

$$\Phi = \mu_0 H L h = \frac{\mu_0 L h}{W} \times I \quad (16)$$

so the inductance is

$$L = \frac{\mu_0 L h}{W}. \quad (17)$$

The capacitance, on the other hand, can be computed using the well-known equation for a parallel plate capacitor

$$C = \frac{\varepsilon_r \varepsilon_0 CW}{h}. \quad (18)$$

If the cutoff frequency is estimated as $f_c = (1)/(2\pi\sqrt{LC})$ then the following result is obtained:

$$f_c = \frac{1}{2\pi\sqrt{\varepsilon_r \varepsilon_0 L h}}. \quad (19)$$

Notice that the dependence on the width of the plate and the thickness of the dielectric cancel out, and the final result depends only on the length and the dielectric constant. Actually, the product of the angular cutoff frequency and the stripline length $2\pi f_c L = (1)/(\sqrt{\varepsilon_r \varepsilon_0 L h})$ is the propagation speed of light in this medium.

Therefore, the trace can be approximated by an $LC$ low-pass filter with a cutoff frequency given by (19). For a representative PCB (FR4) $\varepsilon_r = 4.7$, then the cutoff frequency can be expressed in international units as

$$f_c = \frac{22 \times 10^6}{L}. \quad (20)$$

For example, a 2 cm trace would have a cutoff frequency of 1.1 GHz. It is safe to state that the trace will behave resistively at least up to one decade below the cutoff frequency, in our example 110 MHz. It is concluded that, for all practical purposes, the parasitic dynamic components of the PCB trace will not affect the measurement of the output current. Moreover, there are bypass capacitors in the microprocessor socket cavity and in the microprocessor package which are orders of magnitude larger than the trace capacitance and justify ignoring the high frequency dynamics of the trace.

Another potential source of error is the fact that in a practical layout the $V_o$ node is spread since there are many output capacitors in parallel. This is especially the case in multi-phase buck converters, where the phases are kept apart for thermal considerations. The actual output trace is a wide plate of copper. The lumped resistor model might not be adequate due to the difference in the current density in different portions of the plate, which varies during transients. This can be mitigated by measuring the voltage at $V_o$ using the Kelvin sensing technique with a passive resistor network, so as to average out the voltage at different points in the plate. The technique is illustrated in Fig. 6 for a three-phase VRM.

Finally, in a multi-phase buck converter, and under the assumption that the phase currents are balanced and the adaptation is slow enough to ignore transients, the signal $u(t)$ can be obtained from the switching node of any phase.

IV. EXPERIMENTAL RESULTS

A prototype breadboard implementing the circuit in Fig. 5 was built using standard off-the-shelf parts. A simplified schematic of the breadboard is shown in Fig. 7, and the main component values are shown in Table II. Notice that the factor
$k$ is implemented by changing the ratio of resistors $R1$ and $R2$. The breadboard was connected to the 3-phase VRM evaluation board FAN5019-3A of Fairchild Semiconductor, whose main characteristics are listed in Table III.

The measurements were taken under the following conditions. The VRM board operated independently of the estimation circuit, whose inputs were the voltage across $R_{in}$, the switching node voltage $V_{sw}$, and the voltages at the trace resistance ends $V_o$ and $V_{ref}$ (Fig. 7). The load current was set by an electronic load in the range from 5 A to 50 A in increments of 2.5 A. For each value, the estimated load current was read at the output of U6 and compared with the actual load current. All the measurements were performed at dc.

Results are summarized in Fig. 8. The left-hand side of the figure shows absolute data. The solid line corresponds to the diagonal, which would indicate an estimate that matches the actual current. The squares represent the measured data without any compensation for reverse recovery time, i.e., without adjusting the input current reference gain $(k = (R2)/(R1) = 1)$. Each data point corresponds to a measurement taken after the adaptive estimator has fully converged. The diamonds represent measured data points taken after trimming the gain in the input current path, accounting for the current loss due to reverse recovery. The trimming was done based on empirical observations; however, the gain introduced agrees very well with the gain computed using (10) based on the MOSFET datasheet. The gain was modified by changing $R1$ to 34 KΩ and $R2$ to 32 KΩ, giving $k = (R2)/(R1) = 0.94$. The computed value from the datasheet was $k = 0.93$. The curves on the right-hand side show the same data, but in terms of absolute error and percentage error.

The absolute error remains low for the whole range of load currents, but the relative error is high at light load. At load values below 5 A, the integrator in the estimation circuit starts to drift and may saturate. This is reasonable because the signal level is too low to provide enough information, and the offset voltage of the amplifiers start to dominate the signal. The same situation arises if the converter enters DCM at light load. Although
the absolute error in the current estimate is small, it is desirable to avoid this drift so that the integrator value is correct when the load steps up to a moderate or high value. For these reasons, the integration should be stopped at light load. As previously discussed, this is straightforward with a digital integrator. From the results shown in Fig. 8, a threshold of 20 A would guarantee an estimation error below 2%. To achieve this, $R_t$ should be calibrated during operation at load currents above the threshold, and the calibration should be frozen at load currents below the threshold. Notice that, while the adaptive loop is frozen, the CSA still senses the output current with a constant gain, so the current measurement at light load is still accurate.

The architecture of the estimation circuit allows for an efficient mixed-signal implementation, in which the integration can be performed digitally, with the ability to stop the integration without drift, while the signal conditioning is performed in the analog domain.

V. CONCLUSION

This paper describes a method that allows for an efficient and accurate measurement of the output current in a buck converter. This enables a VRM application to follow the load-line with precision, and to use output current feedforward for a fast transient response.

The method uses the PCB trace resistance at the output of the converter as a sensing element. A slow adaptive loop estimates the gain of the sensing amplifier based on the dc relationship between the output current and the input current, which is measured with a precision sense resistor. The effect of transients and switching non-idealities are quantified and included in the method derivation.

A breadboard was constructed and experiments show a precision better than 2% for currents above 20% of the rated maximum. The adaptation loop should never operate at low currents to avoid drifts in the estimate because of the low signal level compared to the voltage offset of the amplifiers. The estimated current however is accurate for the whole operating range.

Although the method presented makes emphasis on tuning the resistance of the PCB trace, it could be equally used to tune any other sense resistance located in series with the output current or the inductor current, including inductor sensing.

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