

Selective Active Filtering for Four-Wire Loads: Control and Balance of Split Capacitor Voltages

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Abstract - This paper presents a controller for the DC voltages on the split capacitor topology for a four-wire selective active filter. A simple model for the dynamics of the two capacitor voltages is derived under the assumption of time-scale separation between the dynamics of the inverter currents and the capacitor voltages. The controller proposed is based on physical principles and can be easily integrated with existing four-wire active filter controllers based on instantaneous reactive power (p-q) theory. Simulations and experimental results illustrate the benefits of the solution proposed.

I. INTRODUCTION

Selective active filters are used for compensating perturbations introduced by nonlinear loads in the utility network in the form of reactive power and harmonic distortion. In the case of unbalanced loads, a homopolar current is also introduced in the neutral wire. In order to eliminate this undesirable current, a four-wire selective active filter can be used, either by adding a fourth leg to a voltage source inverter (VSI) or by using the split capacitor topology. The latter is a more economical solution but presents the challenge of controlling both the total DC voltage and the voltage balance between the two capacitors.

Previous works have shown ways to control shunt active selective filters [1] [2] (series and parallel methods) depending on the selected control type [3]. These works are typically about three-wire circuits, where homopolar currents are not considered. From the expression of homopolar currents as a sequences function [4] shown in (1), it is evident that channels $i_\alpha(t)$ and $i_\beta(t)$ are completely decoupled from $i_o(t)$. In particular, homopolar channel $i_o(t)$ only depends on homopolar harmonic components I_{0n} .

$$i_\alpha(t) = \sum_{n=1}^{\infty} \sqrt{3}I_{+n} \sin(w_n t + \delta_{+n}) + \sum_{n=1}^{\infty} \sqrt{3}I_{-n} \sin(w_n t + \delta_{-n}) \quad (1)$$

$$i_\beta(t) = -\sum_{n=1}^{\infty} \sqrt{3}I_{+n} \cos(w_n t + \delta_{+n}) + \sum_{n=1}^{\infty} \sqrt{3}I_{-n} \cos(w_n t + \delta_{-n}) \quad (2)$$

$$i_o(t) = \sum_{n=1}^{\infty} \sqrt{6}I_{0n} \sin(w_n t + \delta_{0n}) \quad (3)$$

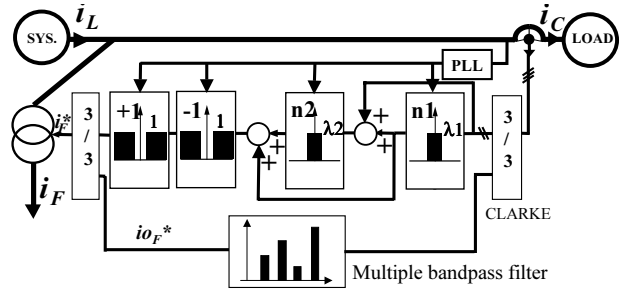


Fig. 1. Selective filtering scheme including the homopolar channel.

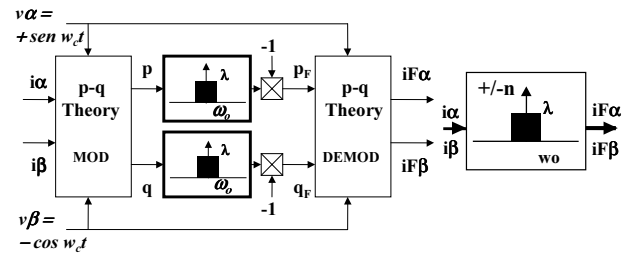


Fig. 2. Selective filter basic cell (SFBC) and its symbol.

Therefore, filtering the homopolar component can be achieved by adding a separate filter to the homopolar channel as shown in Fig. 1. This selective filtering scheme was proposed in [5] and is based on the selective filter basic cell (SFBC) [6] [7] shown in Fig. 2.

An alternative way of controlling a four-wire shunt active filter was presented in [8], in which a nonlinear model-based controller is proposed. There are, however, no clear guidelines for selecting the controller parameters.

This paper extends the results in [5] by presenting a detailed analysis of the DC voltages regulation loop. A small-signal dynamic model is derived in Sec. II. The model shows that the dynamics of the total voltage and the dynamics of the difference between the two capacitor voltages are decoupled, so the design of the controller is simplified. Simulation and experimental results are presented in Sec. III.

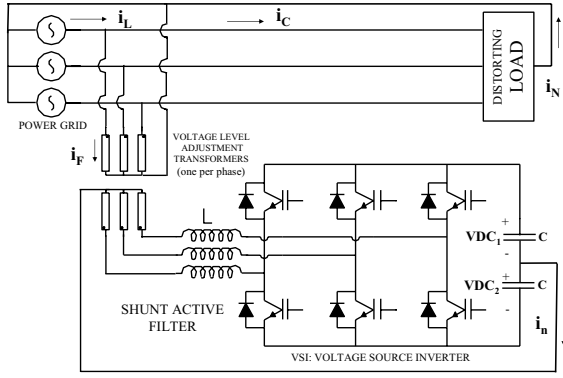


Fig. 3. Four wire VSI with split DC bus.

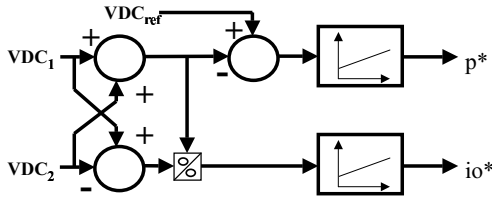


Fig. 4. V_{DC} and balance control strategy.

II. CONTROL OF THE DC VOLTAGES

A. Control Strategy

The four-wire VSI used is shown in Fig. 3. In order to control the total voltage $V_{DC} = V_{DC1} + V_{DC2}$ and to balance voltages V_{DC1} and V_{DC2} , a new decoupled strategy was proposed in [5]. The controller is shown in Fig. 4. The compensation signals p^* and i_o^* are utilized as shown in Fig. 5.

This control strategy is based on physical concepts. In order to control V_{DC} , active power (in fact instantaneous active power \bar{p}) is subtracted or added to the busbar. This is achieved by injecting the p^* control signal in the p channel of the last

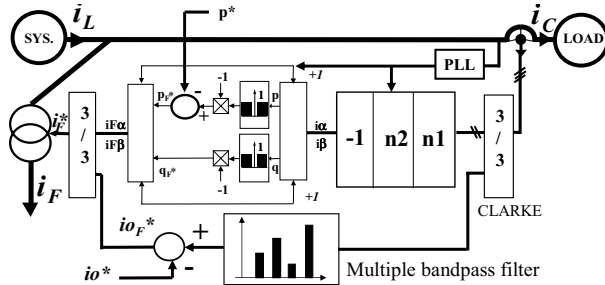


Fig. 5. Complete four-wire selective filtering control strategy including control of the DC voltages.

SFBC (labeled as +1) that controls the amount of positive-sequence fundamental current in phase with the grid voltage. On the other hand, in order to balance V_{DC1} and V_{DC2} , i_o^* (in fact \bar{i}_o) is drained from the middle point of the capacitors. For example if the difference between V_{DC1} and V_{DC2} (relative to V_{DC}) increases, the control drains a current i_o^* that tends to increase V_{DC2} and reduce V_{DC1} .

In the next subsection, a simple small-signal model for the dynamics of the DC voltages is derived. It is shown that this control strategy creates two decoupled loops. The model is also shown to be useful for optimizing the performance of the control loop.

B. Analysis of the Control Loop

The dynamics of the capacitor voltages are usually much slower than the dynamics of the VSI currents. Under this assumption, the VSI can be represented as a static mapping from the reference currents to the actual currents. As shown in Fig. 5 the VSI references are the desired filter currents $i_{F\alpha}$, $i_{F\beta}$ and i_{oF}^* , which the inverter is going to follow with an internal current control method that is of no interest in this derivation. Without loss of generality, the p - q transformation can be lumped into the VSI and therefore it can be assumed that the VSI references are actually p_F , q_F and i_{oF}^* . On the other hand, the actual currents on the VSI will affect the capacitor voltages. The outputs of interest for feedback purposes are $V_{DC1} + V_{DC2}$ and $\frac{V_{DC1} - V_{DC2}}{V_{DC1} + V_{DC2}}$ as shown in Fig. 4.

In spite of its complexity, the filtering mechanisms in Fig. 5 are actually of no relevance to the DC voltage control loop. In fact, they are located in the feedforward path so the reference signals they generate can be considered external perturbations with no effect on the performance and stability of the feedback loop. To clarify this concept, the control loop is redrawn as in Fig. 6.

For the purpose of analyzing the feedback loop it is necessary to derive the mappings from the commanded active power and the commanded homopolar current to the VSI currents on the DC side. Then, those currents are applied to the capacitors to derive the output voltages as illustrated in Fig. 7. The total active power at the VSI DC-side can be computed as

$$p_F^* = i_{C1}v_{C1} + i_{C2}v_{C2}. \quad (4)$$

The neutral current is

$$i_n = i_{C1} - i_{C2} \quad (5)$$

where $i_n = \sqrt{3}\bar{i}_o$ (Clarke transformation).

From (4) and (5), the capacitor currents are

$$\begin{aligned} i_{C1} &= \frac{p_F^* + i_n v_{C2}}{v_{C1} + v_{C2}} \\ i_{C2} &= \frac{p_F^* - i_n v_{C1}}{v_{C1} + v_{C2}}. \end{aligned} \quad (6)$$

This implies that the dynamics of the capacitor voltages are

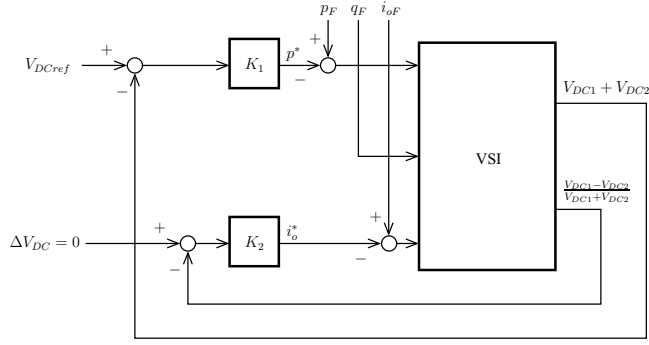


Fig. 6. DC voltages control loop.

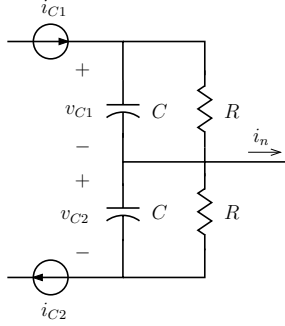


Fig. 7. Simplified model of the VSI DC-side.

given by

$$\begin{aligned} C \frac{dv_{C1}}{dt} &= i_{C1} - \frac{v_{C1}}{R} \\ &= \frac{p_F^* + i_n v_{C2}}{v_{C1} + v_{C2}} - \frac{v_{C1}}{R} \\ C \frac{dv_{C2}}{dt} &= i_{C2} - \frac{v_{C2}}{R} \\ &= \frac{p_F^* - i_n v_{C1}}{v_{C1} + v_{C2}} - \frac{v_{C2}}{R}. \end{aligned} \quad (7)$$

Let $x_1 = v_{C1} + v_{C2}$ and $x_2 = v_{C1} - v_{C2}$, then

$$\begin{aligned} C \frac{dx_1}{dt} &= \frac{2p_F^* - i_n x_2}{x_1} - \frac{x_1}{R} \\ C \frac{dx_2}{dt} &= i_n - \frac{x_2}{R} \end{aligned} \quad (8)$$

The equations are nonlinear, so a small-signal model will be derived by linearization. The operation point (noted with capital letters) is given by $X_1 = V_{DCref}$, $X_2 = 0$, $P_F^* = \frac{V_{DCref}^2}{2R}$, and $I_n = 0$. Then the small-signal model is

$$\frac{d}{dt} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} -\frac{2}{RC} & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} \frac{2}{V_{DCref}C} & 0 \\ 0 & \frac{\sqrt{3}}{C} \end{bmatrix} \begin{bmatrix} p_F^* \\ i_o^* \end{bmatrix} \quad (9)$$

where the relationship $i_n = \sqrt{3}i_o^*$ was used. Here, i_o^* is the homopolar current at the inverter side of the transformer. If

the load homopolar current is measured, then the transformer ratio must be considered.

The outputs are defined as $y_1 = x_1$ and $y_2 = \frac{x_2}{x_1}$. The small-signal relationship is then

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & \frac{1}{V_{DCref}} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}. \quad (10)$$

From (9) and (10) the two-input two-output transfer function is

$$H(s) = \begin{bmatrix} \frac{2}{V_{DCref}C} \frac{1}{s + \frac{2}{RC}} & 0 \\ 0 & \frac{\sqrt{3}}{V_{DCref}C} \frac{1}{s + \frac{1}{RC}} \end{bmatrix}. \quad (11)$$

It is then confirmed that this control strategy actually decouples the two loops and the controller design reduces to two standard single-input single-output (SISO) loops with a first-order plant on each.

III. SIMULATIONS AND EXPERIMENTAL RESULTS

In this section simulated results made with Simulink and an experimental validation of the implementation of the control in the DSP TM320F2812 (kit F2812 eZdsp) are shown. The VSI current control is hysteretic at a regular sampling period.

Data: $V_{DCref} = 340V$, $C = 4400\mu F$, grid voltage $U = 380V$, grid frequency $f = 50Hz$, $L = 10mH$. The transformer indicated in Fig. 3 has a ratio of $220 : 55 = 4$. The sample and control frequency was $f_m = 20kHz$ (400 samples for each grid cycle) so $T_m = 50\mu s$. The time delay introduced by the DSP depends on the number of harmonic sequences being filtered, and is equal to $16.2\mu s$ plus $2.8\mu s$ per homopolar sequence and $3.2\mu s$ per positive or negative sequence.

Having in mind the commutation losses, this sampling and control frequency is equivalent to a $f_m = 20kHz/2 = 10kHz$ averaging PWM current control.

Figure 8 shows the selective filter operation for a dimmerized resistive load. The line current is shown before and after applying the filter. Three different configurations of the selective filter are shown: filtering all harmonics (up to the 17th), filtering only 5th and 7th harmonics, and filtering only the homopolar multiples-of-3 harmonics. No passive filters were used in this experiment.

The small-signal model (11) is validated with a simulation of the DC voltage response to a step in the reference voltage. The PI controllers were tuned to achieve a bandwidth of $10Hz$ and a phase margin of 45° , using standard techniques based on the small-signal model. The bandwidth was selected such that the voltage regulation loops do not interfere with the proper functioning of the filter; a justification for this is included in the appendix.

The output of the small-signal model is compared to that of a full switched model and experimental results in Fig. 9. The correlation between the models and the experimental results is very good.

Figure 10 shows the responses of both the total voltage $V_{DC1} + V_{DC2}$ and the difference $V_{DC1} - V_{DC2}$ to a step in

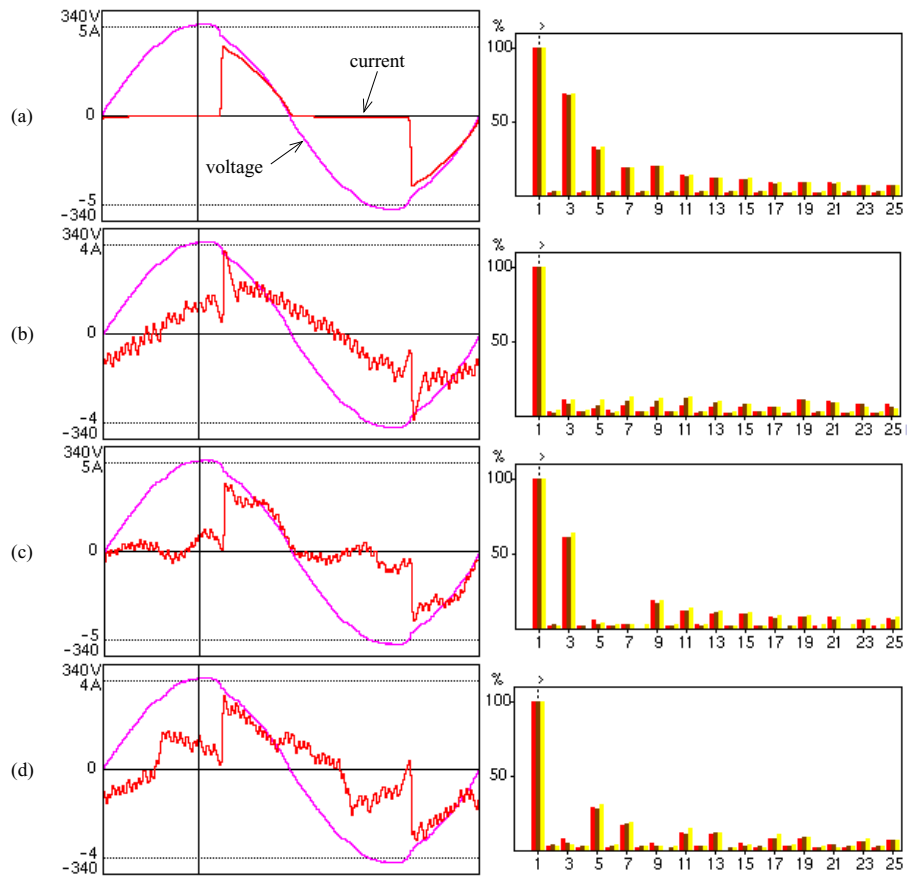


Fig. 8. Load current and selective filtering. Left: voltage and current waveforms; right: line current spectrum. (a) Load current without filtering. (b) Filtering all harmonics up to the 17th. (c) Filtering 5th and 7th harmonics. (d) Filtering homopolar multiple-of-3 harmonics.

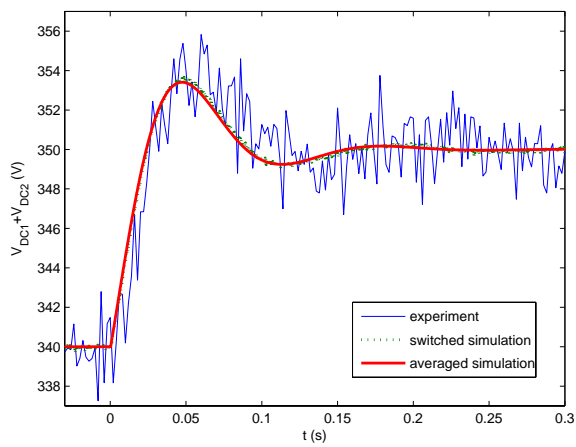


Fig. 9. Step response of the total voltage $V_{DC1} + V_{DC2}$ to a change in the reference value. The small-signal model is compared with a switching model and experimental results.

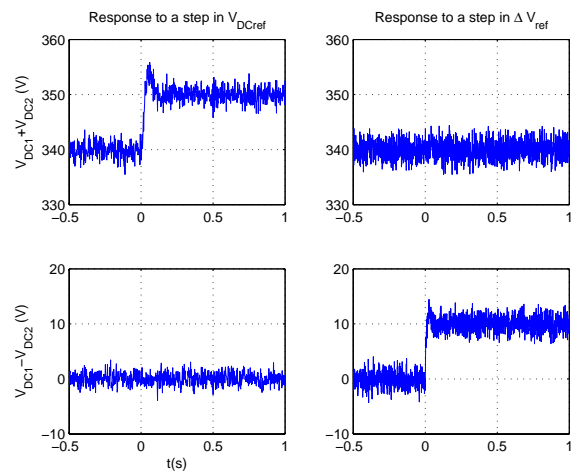


Fig. 10. Step response of the two voltage loops. This experiment shows the decoupling as predicted by the model.

the reference for each loop. The decoupling between the two becomes very clear, in agreement with the model (11).

In Figs. 9 and 10, the experimental voltage shown was acquired with the DSP that introduces noise due to the signal conditioning circuits.

IV. CONCLUSIONS

This paper presents a controller for the DC voltages on the split capacitor topology for a four-wire selective active filter. The main contribution of the paper is the derivation of a small-signal model for the dynamics of the DC voltages in the two capacitors. This model enables the definition of the controller parameters using standard techniques for LTI SISO systems. The benefits of this approach are illustrated with simulations and experimental results. Further, the appendix presents a theoretical justification for selecting the bandwidth of the voltage control loops, also illustrated with experimental results.

APPENDIX

This appendix shows that, under normal operation, the voltage at the capacitors have a ripple which has a frequency that depends on the current harmonic sequences being filtered. The results included in this appendix are useful to define the bandwidth of the voltage control loops such that they do not interfere with the normal filter operation.

First, harmonic expressions for power and homopolar current are derived. Next, the effect of the oscillatory part of these expressions on the capacitor voltages is derived.

The three-phase power in a four-wire system is

$$p3 = p_0 + p \quad (12)$$

where p is the instantaneous power as defined in the $p - q$ transformation, and p_0 is the instantaneous homopolar power.

In steady-state, the instantaneous values p_0 and p have average values of \bar{p}_0 and \bar{p} respectively. Then, the oscillatory values \tilde{p}_0 and \tilde{p} are defined such that

$$p_0 = \bar{p}_0 + \tilde{p}_0 \quad (13)$$

$$p = \bar{p} + \tilde{p} \quad (14)$$

Expressions for \bar{p}_0 , \tilde{p}_0 , \bar{p} and \tilde{p} as a function of the harmonic sequences (positive, negative and homopolar) of voltage and current in the three-phase system were presented in [4], [9] and reproduced here:

$$\bar{p}_0(t) = \sum_{n=1}^{\infty} +3V_{0n}I_{0n} \cos(\phi_{0n} - \delta_{0n}) \quad (15)$$

$$\begin{aligned} \tilde{p}_0(t) = & \quad (16) \\ & \sum_{\substack{m=1 \\ m \neq n}}^{\infty} \left\{ \sum_{n=1}^{\infty} 3V_{0m}I_{0n} \cos[(w_m - w_n)t + \phi_{0m} - \delta_{0n}] \right\} \\ & - \sum_{m=1}^{\infty} \left\{ \sum_{n=1}^{\infty} 3V_{0m}I_{0n} \cos[(w_m + w_n)t + \phi_{0m} + \delta_{0n}] \right\} \end{aligned}$$

$$\begin{aligned} \bar{p}(t) = & \sum_{n=1}^{\infty} 3V_{+n}I_{+n} \cos(\phi_{+n} - \delta_{+n}) + \\ & \sum_{n=1}^{\infty} 3V_{-n}I_{-n} \cos(\phi_{-n} - \delta_{-n}) \quad (17) \end{aligned}$$

$$\begin{aligned} \tilde{p}(t) = & \quad (18) \\ & \sum_{\substack{m=1 \\ m \neq n}}^{\infty} \left\{ \sum_{n=1}^{\infty} 3V_{+m}I_{+n} \cos[(w_m - w_n)t + \phi_{+m} - \delta_{+n}] \right\} \\ & + \sum_{\substack{m=1 \\ m \neq n}}^{\infty} \left\{ \sum_{n=1}^{\infty} 3V_{-m}I_{-n} \cos[(w_m - w_n)t + \phi_{-m} - \delta_{-n}] \right\} \\ & - \sum_{m=1}^{\infty} \left\{ \sum_{n=1}^{\infty} 3V_{+m}I_{-n} \cos[(w_m + w_n)t + \phi_{+m} + \delta_{-n}] \right\} \\ & - \sum_{m=1}^{\infty} \left\{ \sum_{n=1}^{\infty} 3V_{-m}I_{+n} \cos[(w_m + w_n)t + \phi_{-m} + \delta_{+n}] \right\} \end{aligned}$$

where $w_k = kw$ is the k -th harmonic frequency, V_{+k} , V_{-k} and V_{0k} are the amplitudes of the positive, negative and homopolar k -th harmonic sequences respectively (same notation for currents), and ϕ_* and δ_* are the angles for the corresponding harmonic sequence component for voltages and currents respectively.

Finally, the homopolar current is expressed in terms of the corresponding homopolar sequences:

$$i_0(t) = \sum_{n=1}^{\infty} \sqrt{6}I_{0n} \sin(w_n t + \delta_{0n}) \quad (19)$$

A. Homopolar sequence

In case of using the inverter to filter a unique homopolar sequence of index n , from (19) the current can be expressed as

$$i_0(t) = \sqrt{6}I_{0n} \sin(w_n t + \delta_{0n}) \quad (20)$$

Since there are no positive nor negative current harmonic sequences, from (17) and (18) p is zero which implies $p3 = p_0$. Then, from (15) and (16) $p3$ is

$$\begin{aligned} p3(t) = & 3V_{0n}I_{0n} \cos(\phi_{0n} - \delta_{0n}) \\ & - 3V_{0n}I_{0n} \cos[(w_n + w_n)t + \phi_{0n} + \delta_{0n}] \quad (21) \end{aligned}$$

Assuming the inverter has only an inductive load (decoupling impedance between the inverter and an ideal electric network) and setting arbitrarily $\delta_{0n} = 0$, then $\phi_{0n} = \pi/2$. The final expressions for the homopolar current and the power are

$$i_0(t) = \sqrt{6}I_{0n} \sin(w_n t) \quad (22)$$

$$p3(t) = -3V_{0n}I_{0n} \cos[(2w_n t) + \pi/2] \quad (23)$$

For example, if $n = 3$ (filtering the third harmonic of the homopolar) then i_0 has a 3rd harmonic and $p3$ a 6th harmonic. When these inputs excite the system described by (8), the

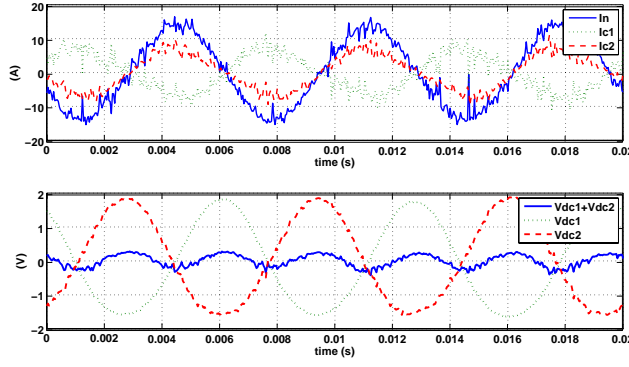


Fig. 11. Voltage ripple generated by filtering the homopolar 3rd harmonic sequence.

resulting voltages v_{C1} and v_{C2} have a dominant ripple with a 3rd harmonic with opposite phases, and the 6th harmonic appears in the total voltage $v_{C1} + v_{C2}$ due to the cancellation of the 3rd harmonic between v_{C1} and v_{C2} . This is illustrated by the experimental results shown in Fig. 11.

B. Positive/negative sequence

In this case the homopolar current is null, so $i_0(t) = 0$.

As in the previous section, the impedance seen by the harmonic sequences is a pure inductance, for a given $I_{\pm n}$ there will be a corresponding $V_{\pm n}$. Then,

$$\bar{p}(t) = +3V_{\pm n}I_{\pm n} \cos(\phi_{\pm n} - \delta_{\pm n}) \quad (24)$$

Setting arbitrarily $\delta_{\pm n} = 0$, then $\phi_{\pm n} = \pi/2$ which results in $\bar{p}(t) = 0$.

Since the three-phase system is ideal, there is only V_{+1} , so from (18)

$$\bar{p}(t) = p3(t) = \pm 3V_{+1}I_{\pm n} \cos[(w_1 \mp w_n)t + \phi_{+1} \mp \delta_{\pm n}] \quad (25)$$

For example, if the harmonic sequence -3 is filtered, then $p3$ will have a frequency component at $w_1 + w_3 = w_4$ which implies an oscillation at $4 \times 50Hz = 200Hz$. Similarly, if the sequence $+3$ is filtered, the oscillation at $p3$ will happen at $100Hz$.

Since $i_0 = 0$, the solution to (8) is simpler than in the previous case and can be computed analytically. Clearly the difference between the voltage on the capacitors is zero: $v_{C1}(t) = v_{C2}(t) = \frac{v_c(t)}{2}$. Let p_M be the amplitude of $p3$ given in (25), and let arbitrarily choose $\phi_{+1} \mp \delta_{\pm n} = 0$. The result is

$$p_M = \pm 3V_{+1}I_{\pm n} \quad (2)$$

$$e(0) = \frac{1}{2} \frac{C}{2} v_c(0)^2 \quad (2')$$

$$v_c(t) = \sqrt{\frac{4}{C} \left[\frac{p_M}{w_1} \sin(w_1 \mp w_n)t + e(0) \right]} \quad (2'')$$

where $v_c(0)$ is the initial value for the total voltage on the DC bus.

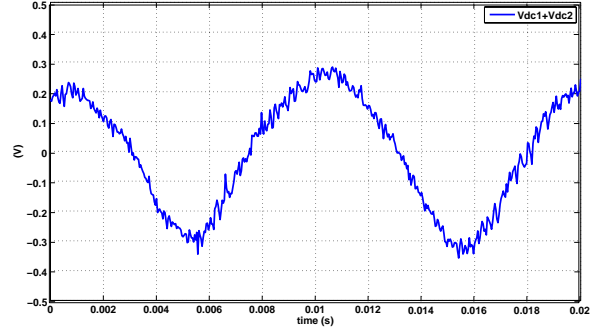


Fig. 12. Voltage ripple generated by filtering the positive 3rd harmonic sequence on $V_{DC1} + V_{DC2}$.

TABLE I
CAPACITOR VOLTAGE RIPPLE FREQUENCY

	$0n$	$+n$	$-n$
$v_{C1} + v_{C2}$	$2n$	$n - 1$	$n + 1$
v_{C1}, v_{C2}	n	$n - 1$	$n + 1$
$v_{C1} - v_{C2}$	n	-	-

This result implies that the ripple at the capacitor voltages has the same frequency as that of $p3$, namely $w_1 \mp w_n$. In Fig. 12 experimental results are shown when filtering the $+3$ harmonic sequence; as expected, a ripple at $100Hz$ appears at the DC bus voltage.

C. Combination of Sequences

Although the system is non-linear, it was shown that to a first-order approximation the dynamics are decoupled. Therefore, superposition can be applied to a certain extent. It is concluded that the harmonic components present in the capacitor voltage ripples will be given by the results of the previous analysis, summarized in Table I.

These results are illustrated with the experimental waveforms shown in Fig. 13, in which both the homopolar 3rd

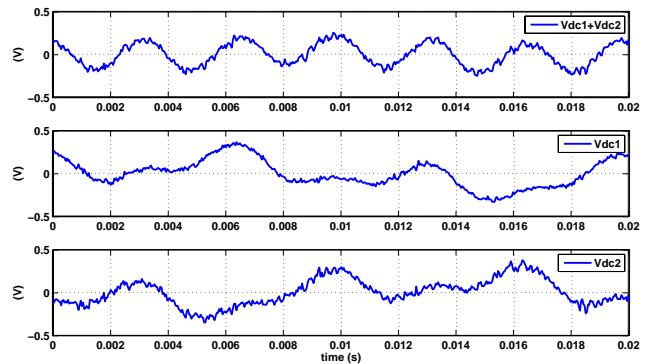


Fig. 13. Voltage ripple generated by filtering the homopolar 3rd and the -5 harmonic sequences simultaneously.

and the -5 harmonic sequences are being filtered. As a consequence, a 6th harmonic appears at the total voltage, and a superposition of a 3rd and a 6th harmonic appears at the individual capacitor voltages.

Concluding, for a given selective harmonic filter, the minimum frequency of the voltage ripple can be computed. This provides an upper bound for the bandwidth of the voltage control loops.

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