RSD CYCLIC ANALOG-TO-DIGITAL CONVERTER

B. GINETTI*, A. VANDEMEULEBROECKE*, P. JESPERS (* sponsored by FNRS)
UNIVERSITE CATHOLIQUE DE LOUVAIN, LABORATOIRE DE MICROELECTRONIQUE
3, PLACE DU LEVANT, 1348 LOUVAIN-LA-NEUVE, BELGIUM

ABSTRACT - A new cyclic analog-to-digital conversion technique is described which allows to achieve high-resolution conversion without the use of accurate voltage comparators.

1. INTRODUCTION
A cyclic converter consists of several functional blocks forming an analog loop shown in Fig. 1. The blocks are:
1) a sample-and-hold device
2) a multiply-by-two amplifier
3) a comparator, and
4) an adder.

Operations performed on the input signal \( X \) to compute its corresponding binary code are based on the "Conventional Restoring" division algorithm (the analog-to-digital conversion can be seen as the division of the input signal \( X \) by the reference \( \text{Ref} \)). The input signal \( X \) is sampled-and-held; it forms the initial partial remainder \( D \) of the division. The signal \( D \) is multiplied by two while going through the amplifier, and the resulting signal \( 2^2D \) is compared to the reference \( \text{Ref} \). This comparison provides the value of the most significant bit \( b_0 \): if the signal \( 2^2D \) is larger than the reference, \( b_0 \) is set to one, and no subtraction is performed. The resulting signal, which can be written \( 2^2D-b_0\text{Ref} \), forms the new partial remainder; it goes through the same operations to compute the second bit of the binary code. The loop is run till the LSB is obtained.

Several electrical devices can be used to implement the functional blocks forming a cyclic A/D converter; for instance, switched-capacitors integrators suit a CMOS realization. Functional blocks nonidealities will affect the operations performed by the analog loop, and limit the accuracy of a cyclic converter.

Many techniques have been developed these last years to reduce or compensate them, such as differential switched-capacitors integrators, or Reference Refreshing cyclic converters. There's still one nonideality which could not be overcome till now: the finite accuracy of the comparator directly limits the accuracy of the converter. For instance, a 16bits A/D cyclic converter working on a 1 volt dynamic range would require a voltage comparator able to detect a 15 microvolts voltage difference. To realize such an accurate device, a very high gain and low noise amplifier must be used: these requirements are usually incompatible with others, such as conversion's speed or required silicon area and power consumption of the circuit.

An accuracy of 13bits seems to be the limit that can be reached by cyclic converters; voltage comparator is the main obstacle to the realization of more accurate devices.

2. RSD CYCLIC CONVERSION
The block diagram of a RSD cyclic A/D converter is shown in Fig. 2; it consists of quite the same analog loop forming a "Conventional Restoring" cyclic converter.

RSD cyclic conversion is based on "SRT" division algorithm. In this algorithm, a RSD (Redundant Signed Digit) binary code is used to represent the ratio between the input signal \( X \) and the reference \( \text{Ref} \): each signed bit can have three values which are -1, 0 and 1 others. To be converted, the input signal \( X \) is sampled-and-held and gives the value of the initial partial remainder \( D \). The signal \( D \) is multiplied by two and the result \( 2^2D \) is compared to half the reference \( 0.5\text{Ref} \) and to its opposite \(-0.5\text{Ref} \). This double comparison gives the value of the most significant signed bit \( b_0 \).
reference, the bit is set to one, and the reference is added to the zero and the signal opposite, the bit is set to zero and the reference is added to the signal 2D.

The resulting signal, which can still be written 2D-bRef, forms the new partial remainder: it runs the loop again to compute next signed bit of the RSD binary code, and so on till the LSB is known.

Table 1 gives the successive values obtained for the partial remainder D while converting an input signal X=0.27Ref, first with a Conventional Restoring converter, and then with a RSD converter. Reference value is one for both converters, and only the first six bits are computed.

<table>
<thead>
<tr>
<th>bit</th>
<th>D 2D</th>
<th>b</th>
<th>D 2D</th>
<th>b</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>0.27</td>
<td>0.54</td>
<td>0.27</td>
<td>0.54</td>
</tr>
<tr>
<td>b2</td>
<td>0.54</td>
<td>1.08</td>
<td>-0.46</td>
<td>-0.92</td>
</tr>
<tr>
<td>b3</td>
<td>0.08</td>
<td>0.16</td>
<td>0.08</td>
<td>0.16</td>
</tr>
<tr>
<td>b4</td>
<td>0.16</td>
<td>0.32</td>
<td>0.16</td>
<td>0.32</td>
</tr>
<tr>
<td>b5</td>
<td>0.32</td>
<td>0.64</td>
<td>0.32</td>
<td>0.64</td>
</tr>
<tr>
<td>LSB</td>
<td>0.64</td>
<td>1.28</td>
<td>-0.36</td>
<td>-0.72</td>
</tr>
</tbody>
</table>

Tab. 1.Conventional Restoring and RSD conversions

3. COMPARATOR ACCURACY REQUIREMENT

A "Conventional Restoring" cyclic converter uses a non-redundant binary code to convert a signal: it means that there is only one binary word that exactly represents the ratio of the signal to the reference. As the value of each bit is set according to the result of a comparison, any comparison error will lead to a wrong binary word: converter accuracy is obviously limited by the accuracy of the comparator.

A RSD converter uses a redundant representation of numbers: a same value can be encoded by different words. For instance, the above value 0.265625 can be represented by any of the following RSD binary words:

\[
\begin{align*}
010001 & \\
1-10001 & \\
01001-1 & \\
1-10011-1 &
\end{align*}
\]

In a RSD conversion, a comparison error will not necessarily lead to a RSD word digital output that is not just one RSD binary code that exactly represents the ratio of the input signal to the reference.

Table 2 illustrates this fact. We have again considered a six bits conversion of a same input signal X=0.27Ref by a Conventional Restoring converter and a RSD converter. We supposed that the comparators used by both converters are affected by an offset value of +0.1 Ref, so that, and so they perform the function:

\[
\text{Out} = 1 \text{ if } \text{In}+ > \text{In} - + 0.1 \text{ Ref}
\]

<table>
<thead>
<tr>
<th>bit</th>
<th>D 2D</th>
<th>b</th>
<th>D 2D</th>
<th>b</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>0.27</td>
<td>0.54</td>
<td>0.27</td>
<td>0.54</td>
</tr>
<tr>
<td>b2</td>
<td>0.54</td>
<td>1.08</td>
<td>0.54</td>
<td>1.08</td>
</tr>
<tr>
<td>b3</td>
<td>1.08</td>
<td>1.16</td>
<td>0.08</td>
<td>0.16</td>
</tr>
<tr>
<td>b4</td>
<td>1.16</td>
<td>1.32</td>
<td>0.16</td>
<td>0.32</td>
</tr>
<tr>
<td>b5</td>
<td>1.32</td>
<td>1.64</td>
<td>0.32</td>
<td>0.64</td>
</tr>
<tr>
<td>LSB</td>
<td>1.64</td>
<td>1.28</td>
<td>-0.36</td>
<td>-0.72</td>
</tr>
</tbody>
</table>

Table 2. Effect of comparison error on Conventional Restoring and RSD conversions.

In the "Conventional Restoring" conversion, a comparison error arises for the second bit decision: due to the comparator offset, the signal 2D=1.08 is not seen larger than the reference Ref=1, and the bit b2 is set to zero instead of one. This error leads to the digital output [001111], which represents the value 0.234375: it is more than a LSB smaller than the exact value 0.27 (LSB=2^-0.015625).

In the RSD conversion, a comparison error arises for the first bit decision: the signal 2D=0.54 is not seen larger than half the reference 0.5Ref=0.5, and the first signed bit is set to zero instead of one. This error leads to the digital output [01001-1]: it represents the value 0.65625, which is the correct rounded approximation of the input signal X!

The difference between the sensitivity of the two converters to comparators unaccuracy clearly appears if we consider the effect of a comparison error on the partial remainder D:

- any comparison error makes the partial remainder of the "Conventional Restoring" conversion diverge: the error on the digital output will be more than a LSB if the resolution increases;
- as long as a signal 2D=Ref can be seen by the comparator larger than 0.5Ref, and a signal 2D=Ref can be seen smaller than -0.5Ref, the partial remainder of the RSD conversion will remain included between the reference and its opposite: the error on the digital output remains less than a LSB whatever is the value of the resolution!

4. CONCLUSION

RSD converters are absolutely insensitive to the accuracy of their comparators: devices of which accuracy is 0.5 volt suits converters working on a one volt dynamic range, whatever is the desired resolution! Comparators, which are critical components for "Conventional Restoring" converters, can be implemented by using very simple electrical circuits such as Schmidt trigger for a RSD converter.

RSD conversion technique allows the realization of A/D cyclic converter more accurate, faster, and requiring less area on Silicon.

REFERENCES