A HIGH COMPLIANCE CMOS CURRENT SOURCE FOR LOW VOLTAGE APPLICATIONS

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ABSTRACT
This paper presents a novel CMOS current source suitable for low voltage applications. The new design shows better compliance voltage than the simple two transistor current mirror while offering improved accuracy and output impedance, featuring 140kΩ output resistance at an output voltage of 30mV and output current of 30pA. The circuit has been manufactured in a 0.25μm, 2.5V power supply digital CMOS process from STMicroelectronics.

1. INTRODUCTION

The current source is, without any doubt, one of the most important building blocks in modern analog applications. This component becomes crucial for low voltage applications where the output voltage compliance of any current mirror must be kept to the minimum value of one saturation voltage, $V_{OS}$, in order to maximize the available signal swing for the remaining circuitry. For this reason, the designer is constrained to use tail sources with one single transistor at the output stage and any cascode-based current source [1][2] is generally ruled out of the final topology choice. However, if the output transistor is required to work at the edge of the transition between the saturation and triode region and below, where its output impedance can quickly degrade, this may impact other performances of the biased circuit such as common mode rejection ratio, and unity gain frequency (due to significant bias current variation).

Interesting workaround to some of these limitations have already been proposed in [3], [4], [5] and [6]. But solution [3], implementing a control circuitry with two feedback loops, one of them positive, needs proper compensation, while the other solutions have more than one transistor in the output path or do not solve the problem of lowering the working output voltage.

The proposed solution achieves similar performances as those of [3] but it does not need a compensation scheme, which results in a considerable area saving especially, for digital processes, where no dedicated layers with high capacitance/area values are available. Moreover the minimum working output voltage can be made as small as needed with an appropriate sizing of $M_1$, $M_2$ in Fig. 1.

2. HIGH COMPLIANCE CURRENT SOURCE

2.1 Principle of operation

The proposed circuit, shown in Fig. 1, exploits a novel control loop to improve the accuracy, voltage compliance and output resistance of the mirror core.

The control loop is based on a regulated cascode ($M_2$) in series with the input branch driven by a high gain amplifier (OTA) that acts as a follower between the output node and the drain of the reference transistor, $M_1$. For a given reference current, the control circuitry equalizes the drain voltage of the reference ($M_2$) and mirror ($M_1$) device increasing the accuracy of the mirroring operation and, as a consequence, the impedance level seen at the output terminal.

In general, if $M_2$ and $M_1$ are well matched, the accuracy of the mirroring ratio between the reference ($I_{ref}$) and output ($I_{out}$) currents depends on their drain to source voltage difference. For a simple current mirror, if the two transistors are in saturation, we recall that the reference to output current ratio is expressed by:

$$\frac{I_{ref}}{I_{out}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

where $V_{DS1}$ and $V_{DS2}$ are the drain to source voltages of the reference and output transistors and $\lambda$ is the channel length modulation parameter (supposing the two transistor are equally sized). It must be noted that, under typical operating conditions, the difference of the two voltages can be as high as the threshold voltage of the transistors.
voltage of M₂, or the minimum voltage for the drain of M₁, is equal to the overdrive voltage of M₂, thus limiting the voltage dynamic range at the output node.

The proposed current source (Fig. 1), offers an efficient solution to this problem without sacrificing additional voltage compliance. If we assume that the input referred offset of the OTA is equal to ε, the drain voltages, when $V_{DS1}$ is sufficiently lower than $V_{GS1}$, are related each other by the following equation:

$$V_{DS1} = V_{DS2} + \epsilon$$

and the current ratio can now be expressed as:

$$\frac{I_{ref}}{I_{out}} = \frac{1}{1 + \frac{\lambda \epsilon}{1 + \lambda V_{DS2}}}$$

With a careful design of the feedback amplifier the accuracy of the mirror can be greatly improved and the current ratio can be precisely controlled throughout the voltage range for which the control loop remains active.

The simple PMOS amplifier shown in Fig. 2 has been used in order to guarantee the correct control loop operation at voltage levels close to ground. On the other hand, such a simple topology does not require the OTA having higher input common mode voltage than the minimum $V_{CM}$ (referring to Fig. 1).

With the topology shown in Fig. 1, the voltage compliance of the proposed mirror can be higher than the one of the simple mirror thus allowing for very low voltage operation modes.

The circuit, in fact, performs efficiently the mirroring operation when the two transistors, M₁ and M₂, work in both saturation and triode region.

In this latter case, an upper bound is set on the maximum input current since, for very small $V_{GS}$ values, the gate voltage of M₁₂ rises according to the following equation:

$$V_{GS\min} = \frac{I_{ref}}{\mu C_{ox}(W/L)_{1,2} V_{DS}} + V_{TH,1}$$

Therefore, in order to properly design the circuit for a given $V_{DS\min}$ and $I_{out}$, $(W/L)_{1,2}$ should be chosen to set the maximum gate voltage of $V_{GS\min}$, to guarantee that the circuitry which provides the reference current works properly.

Once the ratio has been chosen it is possible to derive the minimum gate to source voltage of $M_{1,2}$, $V_{GS\min}$ at the onset of saturation:

$$V_{GS\min} = V_{TH} + \sqrt{2 V_{DS\min} (V_{GS\max} - V_{TH})}$$

When output voltage, $V_{DS1}$, approaches this value $M_1$ is eventually driven into linear region and the circuit tends to behave like a simple current mirror.

### 2.2 Small signal analysis

The DC small signal equivalent circuit is shown in Fig. 3, below:

![Figure 3. Small signal DC circuit](image)

In order to derive the expression for the output resistance of the circuit we make use of its DC, current controlled, 2-port description reported below:

$$\begin{bmatrix} v_o \\ i_o \end{bmatrix} = \begin{bmatrix} A_1 & A_2 \\ A_3 & A_4 \end{bmatrix} \begin{bmatrix} v_i \\ i_i \end{bmatrix}$$

where $A$ represents the OTA DC voltage gain while $A_1=g_{m1}r_{01}$, $A_2=g_{m2}r_{02}$, $A_3=g_{m3}r_{03}$. The matrix elements have been derived in the case that $A_1=A_2$ and no body effect for $M_3$ has been included in the analysis.

It is possible to identify 3 working regions:

a) $M_1$ and $M_2$ are both in triode region and $M_3$ in saturation region, or $V_{DS1}>V_{DS2}>V_{GS1}$.

b) all the three transistors $M_1$, $M_2$ and $M_3$ are in saturation region, or $V_{DS1}>V_{DS2}>V_{GS1}$.

c) $M_1$ and $M_2$ are both in saturation region and $M_3$ is in triode region because the OTA saturates at $V_{DS1}$ and $V_{DS1}>V_{DS2}$ while $V_{GS1}$ tends to $V_{GS1}$.

In the first working region a, $A_1,A_2<1$ and the expression for the output resistance becomes

$$r_{out} = \frac{v_o}{i_o} \bigg|_{i_o=0} = r_{\lambda} \left( \frac{K}{1 + K} A + 1 \right)$$

where $K$ is the value of the product of $A_1,A_2$. The latter equation, together with the one for $V_{GS\min}$, defines the trade-offs between the minimum voltage compliance and the minimum output resistance of the circuit, whereas the accuracy of the mirror operation can be independently set by the feedback control loop.
and, within its working range, is limited only by the quality of the
amplifier of Fig. 2 and by the mirror device mismatches.

In the second working region b, \( A, A_A, A_2, A_3 \gg 1 \) and it can be
easily shown that the output resistance of the proposed current
source is:

\[
r_{\text{out}} = \frac{V_o}{i_o} = r_o (A + 1)
\]

which is \((A+1)\) times the one of the simple current mirror as it is
in the third working region c.

3. SIMULATION AND EXPERIMENTAL RESULTS

The test chip has been fabricated in a 0.25\( \mu \)m digital N-well,
single poly, six metal level CMOS process.

Three different current sources have been implemented with
different devices length for \( M_1 \) and \( M_2 \) (1\( \mu \)m, 0.5\( \mu \)m \& 0.25\( \mu \)m,
respectively) while keeping the W/L constant and equal to 4.

The amplifier used, shown in Fig. 2, is a single stage six
transistor PMOS-input OTA that exhibits a DC gain of about
53dB and more than 75 degrees of phase margin. Its input
common mode range includes the ground level and it has been
biased with a 1\( \mu \)A current.

The process parameters for the adopted technology are
summarized in Tab. 1.

Fig. 4 shows the proposed current source characteristics (i.e., its
output current vs. output voltage) for reference current values
ranging from a minimum of 10\( \mu \)A up to 100\( \mu \)A.

The circuit exhibits an excellent mirroring function well below
the typical \( V_{\text{DSat}} \) of 200-250mV. As shown in Fig. 5, for \( I_{\text{ref}}=30\mu\text{A} \)
the output current remains constant for \( V_{\text{out}} \) down to 23mV when

\( M_1-M_2 \) have W/L=4. Increasing the \( M_1-M_2 \) W/L ratio, the
minimum working output voltage lowers proportionally to 12mV
when \( M_1-M_2 \) W/L=8 and to about 4mV when \( M_1-M_2 \) W/L=24.

For lower values of \( V_{\text{sat}} \), the gate of \( M_1 \) rises above the
compliance of the instrument (set to 2.8V) and the reference
current is limited as well.

As visible in Fig. 6, the output impedance does not remain
constant throughout the whole range of operation.

In the lower voltage range the output resistance decreases because
the gate voltage of \( M_1 \) tends to saturate to \( V_{DD} \). In the middle
voltage range the output resistance reach its maximum value, in
the M\( \Omega \) range, because the circuit is in the working region a and
b where the loop is more effective. In the higher voltage range,
corresponding to the third working region c, the output resistance
tends to the value of the simple current mirror because when the

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**Figure 4.** Comparison between simulated (lines) and measured characteristics (symbols) of the proposed current source (W/L\( M_1, M_2 \)=4/1, \( V_{DD} = 2.5\)V, \( T = 27^\circ\text{C} \))

**Figure 5.** Simulated characteristics of the proposed current source with W/L\( M_1,M_2 \) variable from 4 to 24 (\( V_{DD} = 2.5\)V, \( I_{\text{ref}} = 30\mu\text{A} \), \( T = 27^\circ\text{C} \))

**Figure 6.** Measured output conductance of the proposed current source (W/L\( M_1,M_2 \)=4/1, \( V_{DD} = 2.5\)V, \( I_{\text{ref}} = 30\mu\text{A} \), \( T = 27^\circ\text{C} \))
output of the amplifier saturates the loop is no more effective and, as a consequence, \( V_{DS1} > V_{DS2} \).

The circuit behavior has also been analyzed as a function of temperature as reported in Fig. 7.

The figure shows that the quality of the mirroring operation as a function of temperature is affected only in the range for which the input stage limits the reference current generator, or when \( V_{DS1} \) and \( V_{DS2} \) are very low and \( V_{OS} \) rises towards \( V_{DD0} \). The circuit shows no significant temperature dependency in the working range.

The collected experimental data have been measured using a semiconductor parameter analyzer and reported in Fig. 4, Fig. 6, Fig. 7 which represent respectively: the characteristic \( I_{os} \) vs. \( V_{DD0} \) for different values of \( I_{ref} \), the conductance seen at the output terminal and the dependency of the current source characteristic on temperature.

A close comparison shows that there is a good agreement between simulated and measured values.

Fig. 8 shows a microphotograph of the fabricated test chip.

4. CONCLUSIONS

A novel current source suitable for low voltage applications has been proposed which exhibits better voltage compliance than the simple current mirror, improved accuracy and high output resistance. The operation of the circuit is based on a high gain control loop that can be designed without large area overhead. The developed current source can be incorporated in the design of high performance filters and/or amplifiers operating at fairly low power supply values.

5. ACKNOWLEDGMENTS

Authors thanks Luciano Fumagalli and Chantal Auricchio for support in testing the device.

Figure 8. Test device microphotograph with indicated the different W/L of the transistor M1-M2.

![Figure 8](image)

Table 1. Process Parameters

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.25um P-sub CMOS, 1 polysilicon, 6 metal</th>
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<tbody>
<tr>
<td>PMOS ( V_{th} )</td>
<td>-0.54V</td>
</tr>
<tr>
<td>NMOS ( V_{th} )</td>
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6. REFERENCES


