A 2V Rail-to-Rail Micropower CMOS Comparator

ABSTRACT

The 2V rail-to-rail micropower CMOS comparator offers a maximum dynamic range of 10lg in the presence of a multiphase operational amplifier and the comparator must operate on a supply voltage of 2V or less. The comparator is capable of operating over a temperature range of -40°C to 85°C and is designed for use in low-power applications. The comparator features a high common-mode input range, allowing it to operate with a wide variety of input signals. The device is particularly useful in applications requiring high-speed operation with minimal power consumption.
**A. DESIGN METHODOLOGY**

Fig. 2. Block diagram of the receiver.

![Block Diagram](image)

**Discussion**

The design methodology involves the following steps:

1. **System Specification**: Define the requirements and the specifications of the system.
2. **Component Selection**: Choose appropriate components that meet the design criteria.
3. **Circuit Design**: Design the analog and digital circuits to meet the system requirements.
4. **Simulation and Testing**: Simulate the circuit to verify its functionality and performance.
5. **Prototype Development**: Develop a prototype to test the functionality in a real-world environment.
6. **Integration and Testing**: Integrate the prototype with other systems and test the overall system performance.

**Fig. 2**

The block diagram of the receiver shows the various components and their interconnections. The receiver consists of the following sections:

- **Antenna**: Receives the incoming signal.
- **Low-Noise Amplifier (LNA)**: Enhances the signal strength.
- **Mixers**: Converts the frequency of the signal.
- **IF Amplifiers**: Further amplifies the signal.
- **Demodulator**: Decodes the signal to extract the information.
- **Controller**: Manages the operations of the receiver.

**Conclusion**

The receiver designed using this methodology meets the specified requirements and demonstrates excellent performance in real-world applications.

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**Journal of Solid-State Devices and Circuits**

Vol. 3, No. 1, February 1997

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**Diagram**: Diagram of the receiver's block diagram.
The synthesis procedure followed was as follows:

1. From the total consumption specification, the circuit topology of Fig. 2 is chosen through each transistor was determined.

2. A $\text{V}_{\text{DD}}$ value is chosen for the gates of each transistor. From this value, the following relationships are obtained:
   \[
   L_{\text{DD}} = \frac{V_{\text{DD}}}{2}
   \]
   \[
   L_{\text{SS}} = \frac{V_{\text{DD}}}{2}
   \]
   \[
   L_{\text{OUT}} = \frac{V_{\text{DD}}}{2}
   \]

3. A $\text{V}_{\text{TH}}$ value is chosen for the output of each transistor. The $\text{V}_{\text{TH}}$ value is calculated from the following relationship:
   \[
   \text{V}_{\text{TH}} = \frac{V_{\text{DD}}}{10}
   \]

4. A $\text{V}_{\text{DS}}$ value is chosen for the drain of each transistor. The $\text{V}_{\text{DS}}$ value is calculated from the following relationship:
   \[
   \text{V}_{\text{DS}} = \frac{V_{\text{DD}}}{20}
   \]

5. The gain, speed, and offset are predicted and checked against the desired performance. If they are not acceptable, the values of $\text{V}_{\text{TH}}$, $\text{V}_{\text{DS}}$, and $\text{V}_{\text{DD}}$ are modified until the desired performance is achieved.

6. The resulting circuit is simulated and the measured characteristics are compared with the predicted results. The circuit is modified until the measured characteristics are within acceptable limits.

V. SIMULATED AND MEASURED PERFORMANCES

The main circuit estimated and measured characteristics are shown in Fig. 5. The measured results show that all the expected performance characteristics are met. The circuit is suitable for use in a wide range of applications.

![Fig. 5. Layout of comparator cell and complete chip.](image-url)
Conclusions

Figure 6: True current consumption vs. input common mode voltage

\[ (\text{AV/MP}) = \frac{1}{Z_2} \frac{G_2}{Z_1} \]

References

Acknowledgment

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Table 2: Circuit Characteristics