**Modular ultra low power dc-dc converter with losses reduction using charge recycling.**

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**MOTIVATION**

- Implantable or portable battery
- V.bat: [1.2V ... 4.1V]

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**PROPOSED ARCHITECTURE**

- Based on series of capacitors (Fig 1).
  - Phase T1: capacitor charge from VDD.
  - Phase T2: load connection.
  - The node connected during T2 determines the conversion ratio.
  - The capacitors are rotated in a loop (Fig. 2), so that in steady state the voltage across all of them are approximately equal.
  - Waveforms are shown in Fig. 3.
  - Based on a basic cell (Fig 4).

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**CHARGE RECYCLING TECHNIQUE**

- Recycle the charge from parasitic capacitors that need to decrease its charge (related to top plate of C5 (VC5) in Fig. 3) to those that need to increase its charge (top plate of C4...C1 in Fig. 3).
- Fig. 5 summarizes the process and Fig. 6 shows the reduction of the contribution of parasitic capacitance losses (a.k.a bottom plate losses).

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**RESULTS**

- Fig 7. Efficiency vs. load current (4/5 conv. ratio) with and w.o. parasitic losses reduction technique based on charge recycling.

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**FUTURE WORK**

- Fabrication (2/2013 in 130 nm) and prototype testing.
- Extend the application of the charge recycling principle.

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